

# AT3 BLOCK DIAGRAM

01

## PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : SGND1
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : IN3
- LAYER 7 : SGND2
- LAYER 8 : BOT

04-- 0402 footprint  
 06-- 0603 footprint  
 08-- 0805 footprint  
 12-- 1206 footprint  
 F-- 1% tolerance

**CPU Merom**  
 478P (uPGA)/35W  
 PAG 3, 4

**CPU THERMAL SENSOR**  
 PAG 5

**CLOCK GEN**  
 ICS9LPRS355AGLFT  
 64pinsTSSOP  
 PAG 2

**NORTH BRIDGE**  
 Crestline  
 PAG 7, 8, 9, 10, 11, 12

**NVIDIA G3-64 for 15.4"**  
**NVIDIA G3-128 for 17"**  
 820p FCBGA  
 PAG 15, 16, 17, 18, 19, 20

**HDMI CON**  
 Option for 17" only  
 PAG 26

**DDRII-SODIMM1**  
 DDRII 533,667 MHz  
 PAG 13, 14

**DDRII-SODIMM2**  
 DDRII 533,667 MHz  
 PAG 13, 14

**Cable Docking**  
 TV\_OUT  
 VGA  
 RJ-45  
 CIR/Pwr btn  
 SPDIF Out  
 Stereo MIC  
 Headphone Jack  
 USB Port  
 VOL Cntr  
 PAG 38

**SYSTEM CHARGER(MAX8724)**  
 PAG 41

**SYSTEM POWER MAX8778**  
 PAG 42

**DDR II SMDR VTERM**  
 1.8V/1.8VSUS(TPS51116REGR)  
 PAG 46

**VCCP +1.5V AND GMCH**  
 1.05V(MAX8717)  
 PAG 43

**VGACORE(1.025V)MAX1992**  
 PAG 45

**CPU CORE MAX8771**  
 PAG 44

**SATA - HDD**  
 SATA2  
 Option for 17" only  
 PAG 35

**SATA - HDD**  
 SATA0 150MB  
 PAG 32

**PATA- CD-ROM**  
 PATA (66/100/133)  
 PAG 32

**SOUTH BRIDGE**  
 ICH-8M  
 PAG 21, 22, 23, 24

**USB2.0**  
 Bluetooth PAG 35  
 USB2.0 I/O Ports X3 PAG 32  
 Camera X1 PAG 32  
 Mini PCI-E Card x1  
 Express Card x1  
 Cable Docking x1

**PCI BUS / 33MHz**  
 PCI-E

**Alalia**  
 Mini PCI-E Card  
 PCI Express Mini Card (Wireless LAN/WAN) PAG 39  
 LAN Realtek PCIE-LAN TLE8101E/8111B 10/100/GigaLAN PAG 33, 34  
 Express Card (NEW CARD) PAG 35  
 RICOH RICOH 832 PAG 27, 28

Keyboard Touch Pad PAG 36

CIR PAG 36

Capacitive Sense SW PAG 36

**ENE KBC**  
 KB3920 Bx  
 KB3926 Bx  
 PAG 37, 48

FAN PAG 38  
 Flash PAG 37  
 SPI PAG 37

Two-element microphone PAG 29

Audio Jacks (Phone/ MIC) PAG 29

**AUDIO Amplifier**  
 PAG 30  
 Jack to Speaker PAG 30

**Realtek**  
 ALC 268  
 PAG 29

**MDC DAA**  
 SI3080  
 PAG 31  
 MODEM RJ 11 PAG 33

**Mini PCI-E Card**  
 PCI Express Mini Card (Wireless LAN/WAN) PAG 39

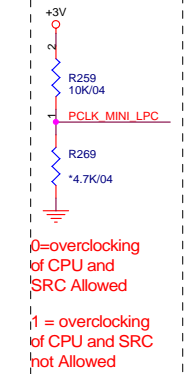
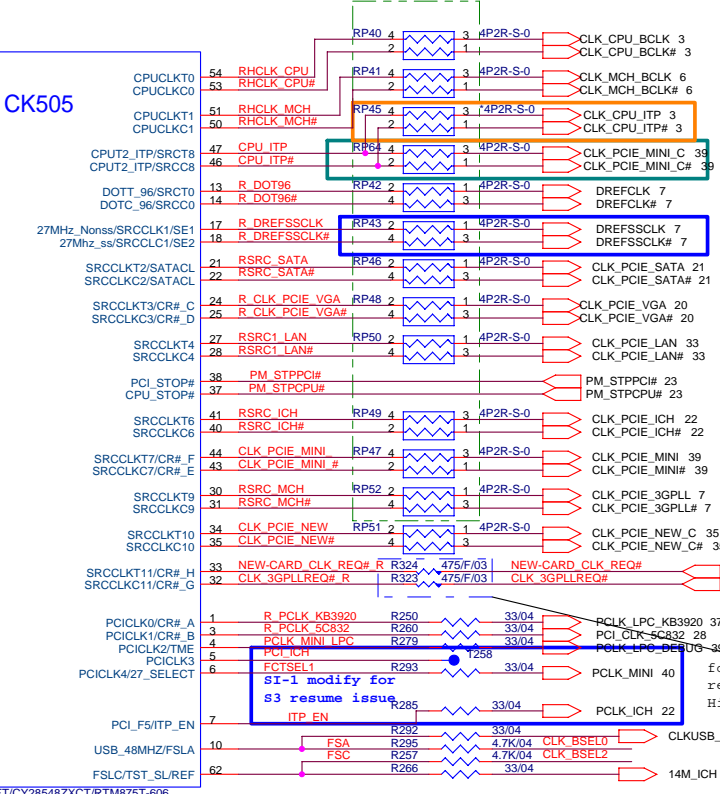
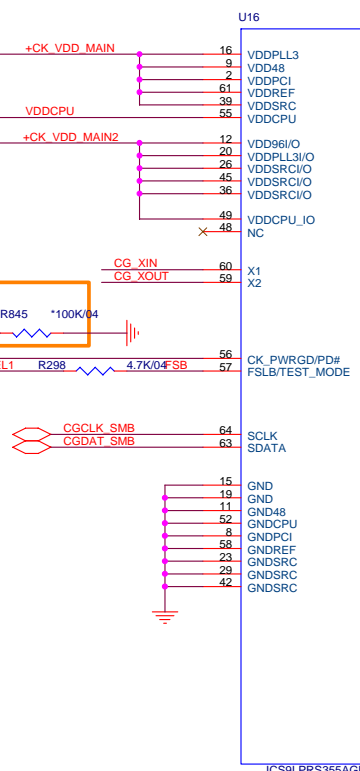
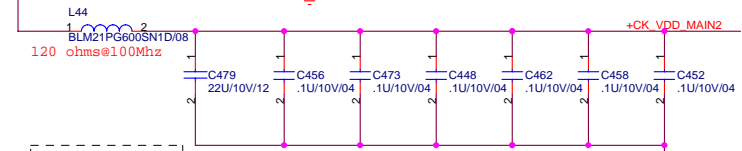
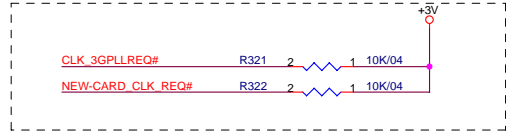
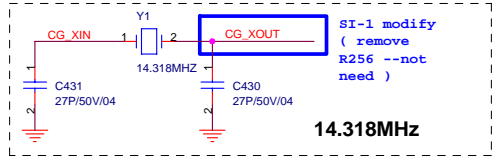
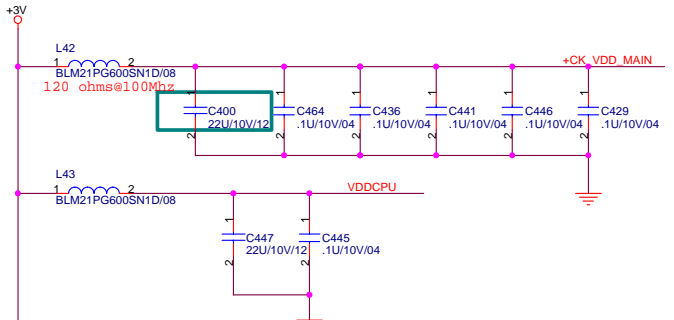
**RJ45**  
 PAG 33

IEEE1394 CONN PAG 28  
 Memory CardReader PAG 27

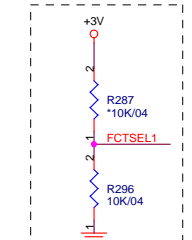
PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD25	INTE#,INTF#	RICOH832
REQ1# / GNT1#	AD22	INTC#,INTD#	MINI PCI for debug



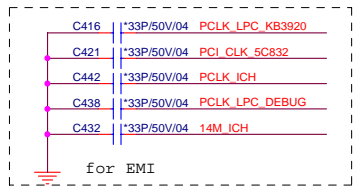
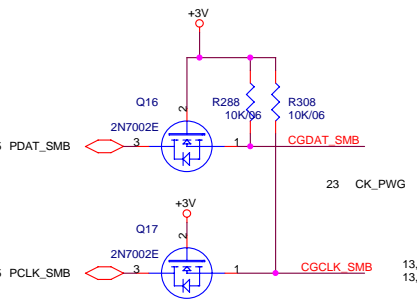
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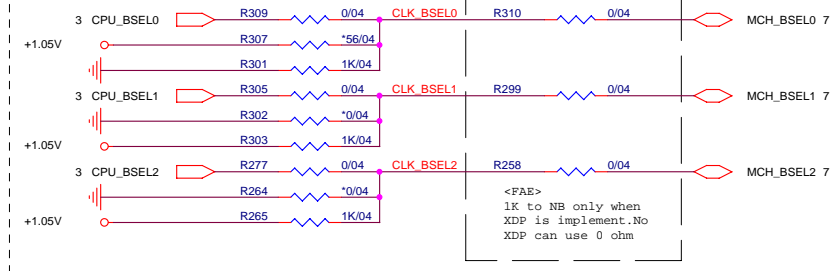
0=overclocking of CPU and SRC Allowed  
1 = overclocking of CPU and SRC not Allowed



0=UMA  
1 = External VGA



### CPU Clock select



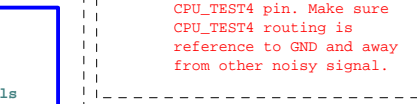
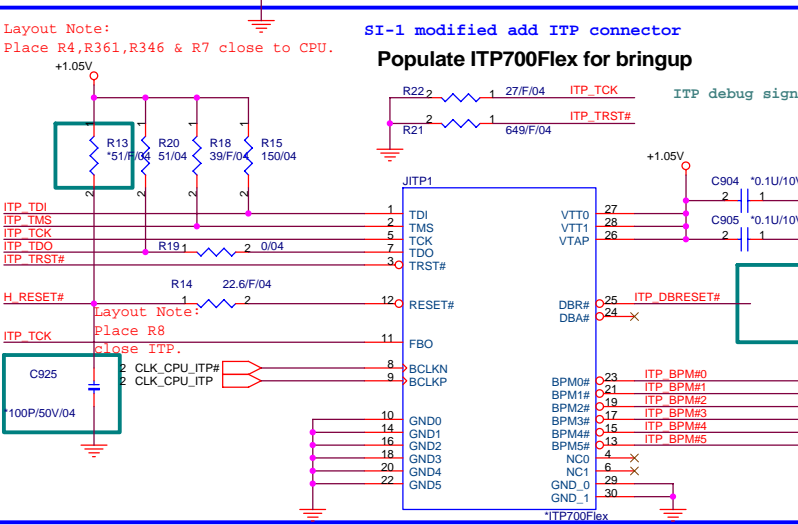
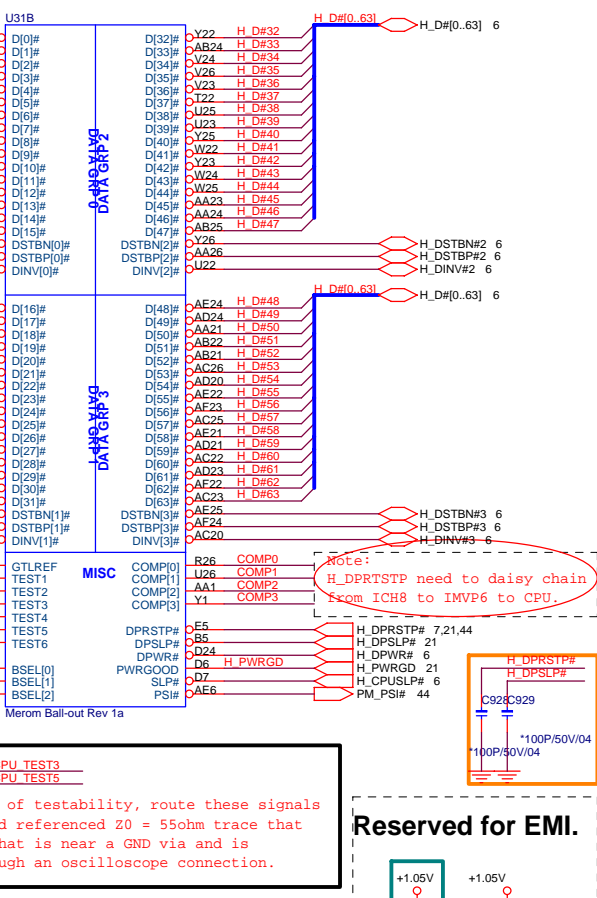
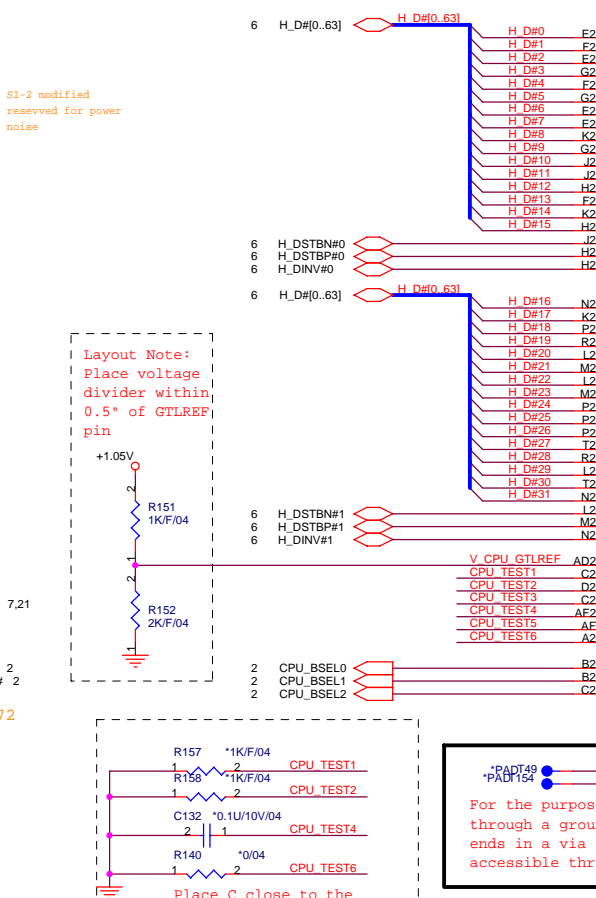
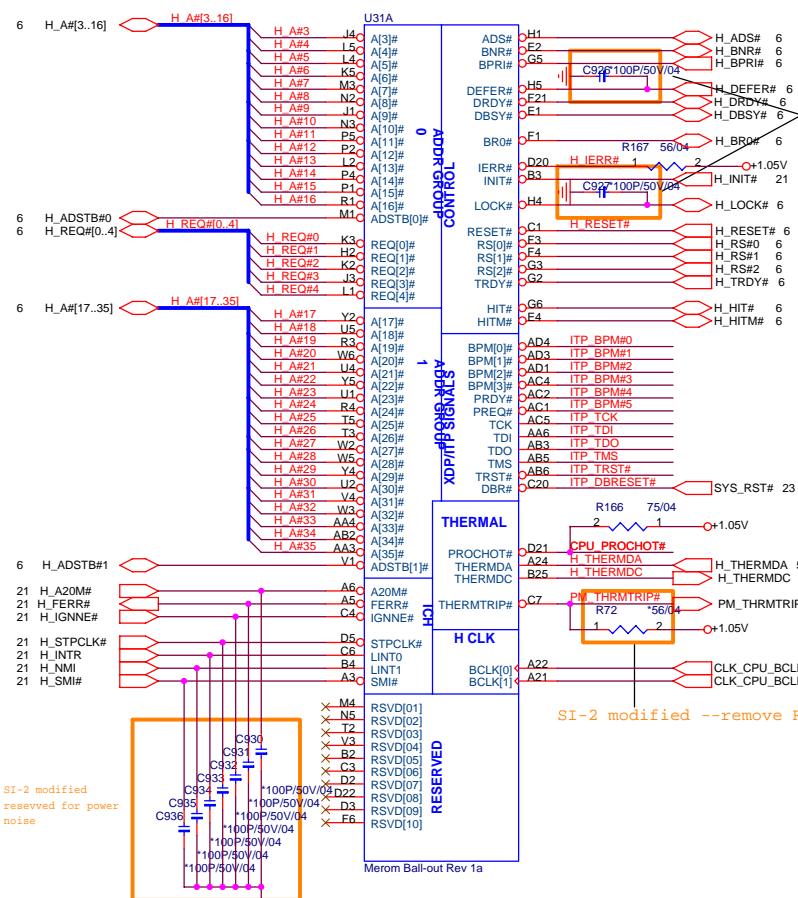
FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

### GCLK\_SEL = FCTSEL1

FCTSEL1 (PIN13)	PIN20	PIN21	PIN24	PIN25
0=UMA	DOT96T	DOT96C	SRCT1/LCDT_100	SRCT1/LCDT_100
1 = External VGA	SRCT0	SRCC0	27Mout-NSS	27Mout-SS

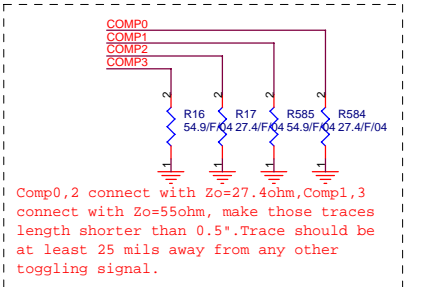


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FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0

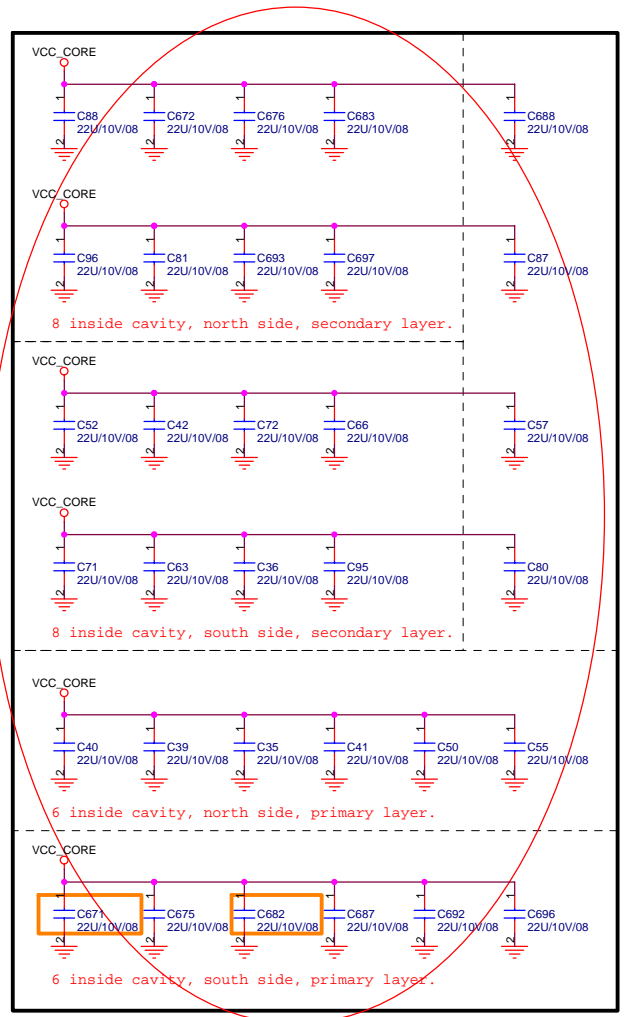
ITP disable guidelines			
Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 ohm +/- 5%	VTT	Within 2.0" of the ITP
TMS	39 ohm +/- 1%	VTT	Within 2.0" of the ITP
TRST#	500-680ohm +/- 5%	GND	Within 2.0" of the ITP
TCK	27 ohm +/- 1%	GND	Within 2.0" of the ITP
TDO	150 ohm +/- 5%	VTT	Within 2.0" of the ITP



Note: Populate R5, R8, C372 & R430 when ITP connector is populated.



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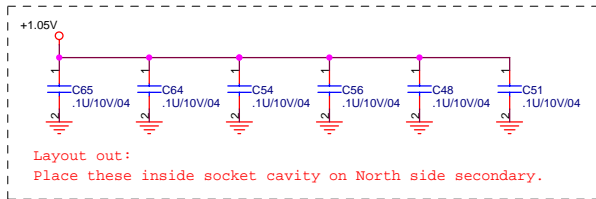


8 inside cavity, north side, secondary layer

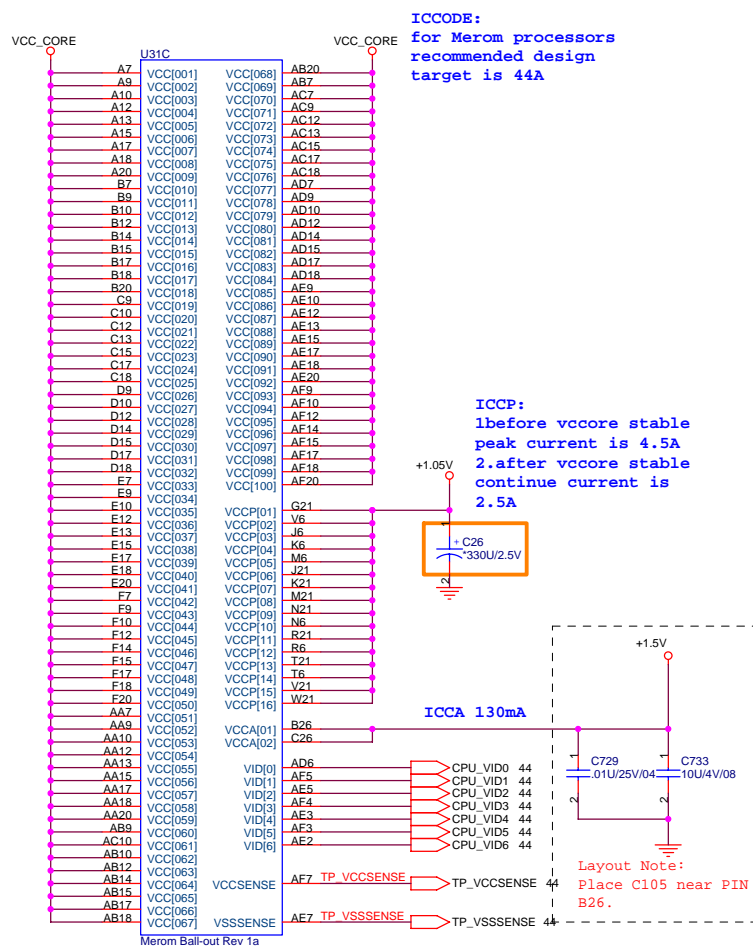
8 inside cavity, south side, secondary layer

6 inside cavity, north side, primary layer

6 inside cavity, south side, primary layer



Layout out:  
Place these inside socket cavity on North side secondary.

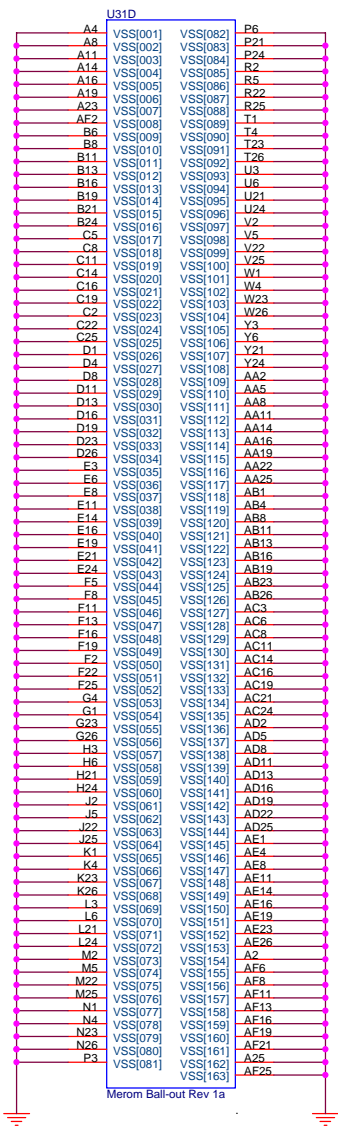


ICCODE:  
for Merom processors  
recommended design  
target is 44A

ICCP:  
before vccore stable  
peak current is 4.5A  
2. after vccore stable  
continue current is  
2.5A

ICCA 130mA

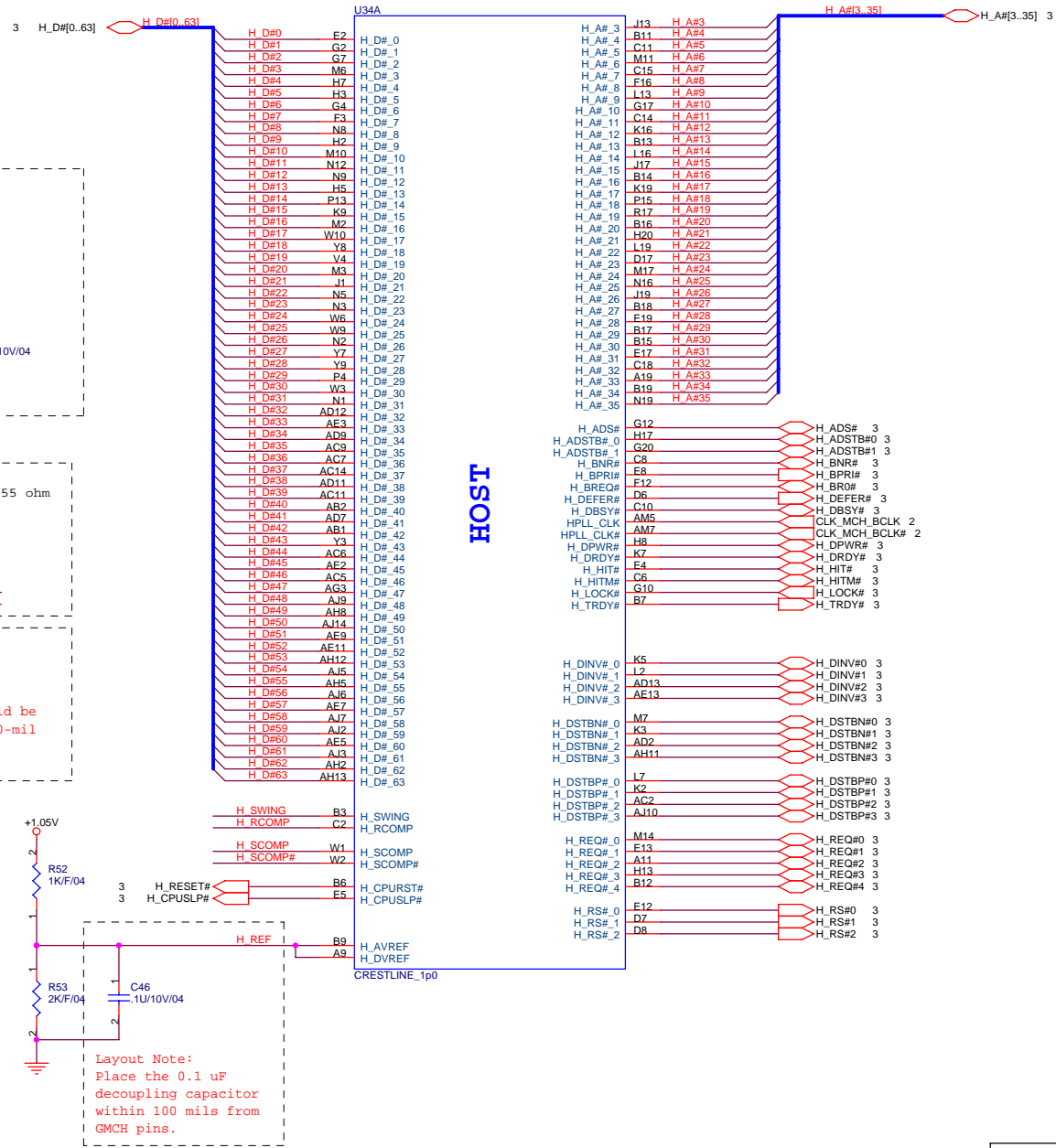
Layout Note:  
Place C105 near PIN  
B26.



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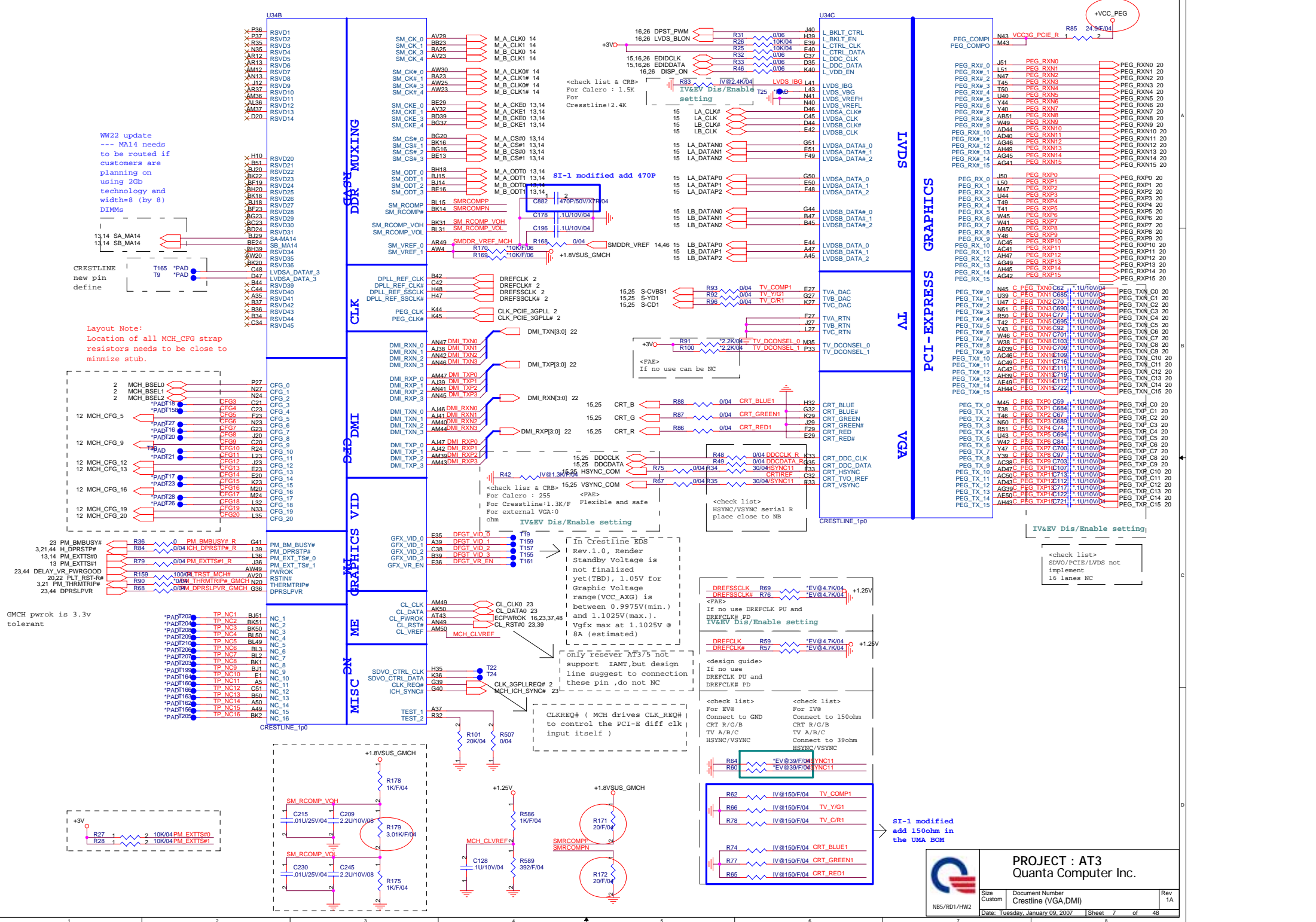
Size Custom	Document Number Merom Processor (POWER)	Rev 1A
Date: Tuesday, January 09, 2007	Sheet 4 of 48	





**HOST**

	<b>PROJECT : AT3</b> Quanta Computer Inc.		Rev 1A
	Size Custom	Document Number Crestline (HOST)	Date: Tuesday, January 09, 2007
Sheet 6 of 46		1A	



Ww22 update  
 --- MA14 needs  
 to be routed if  
 customers are  
 planning on  
 using 2Gb  
 technology and  
 width=8 (by 8)  
 DIMMs

Layout Note:  
 Location of all MCH\_CFG strap  
 resistors needs to be close to  
 minimize stub.

In Crestline BDS  
 Rev.1.0, Render  
 Standby Voltage is  
 not finalized  
 yet(TBD), 1.05V for  
 Graphic Voltage  
 range(VCC\_AGX) is  
 between 0.9975V(min.)  
 and 1.1025V(max.).  
 Vgfx max at 1.1025V @  
 8A (estimated)

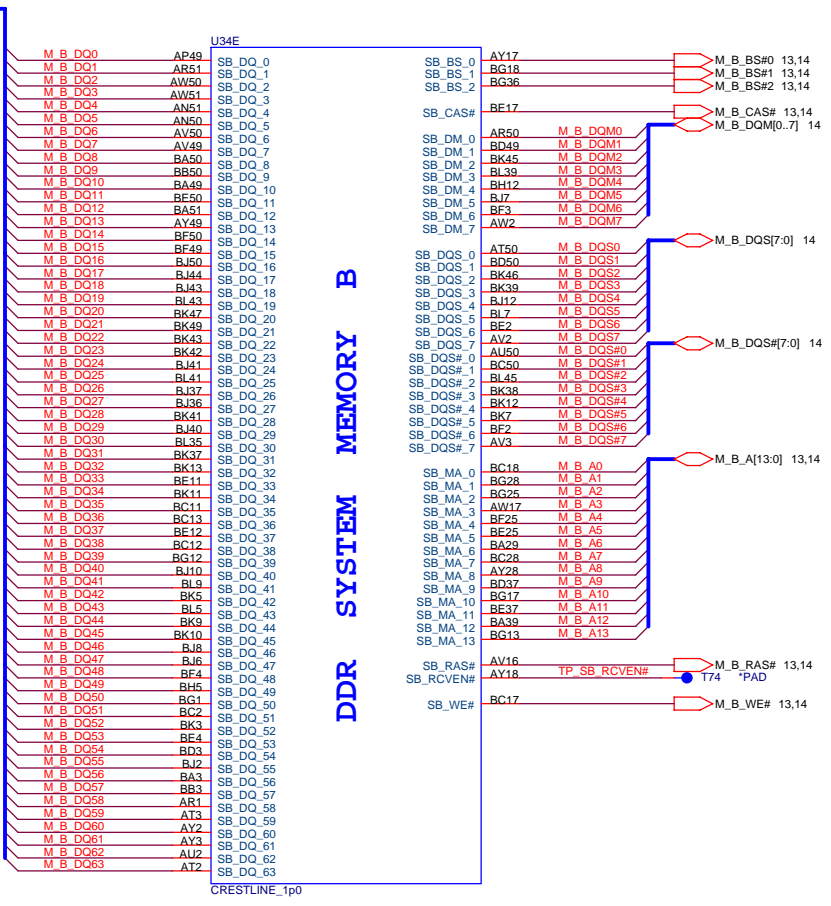
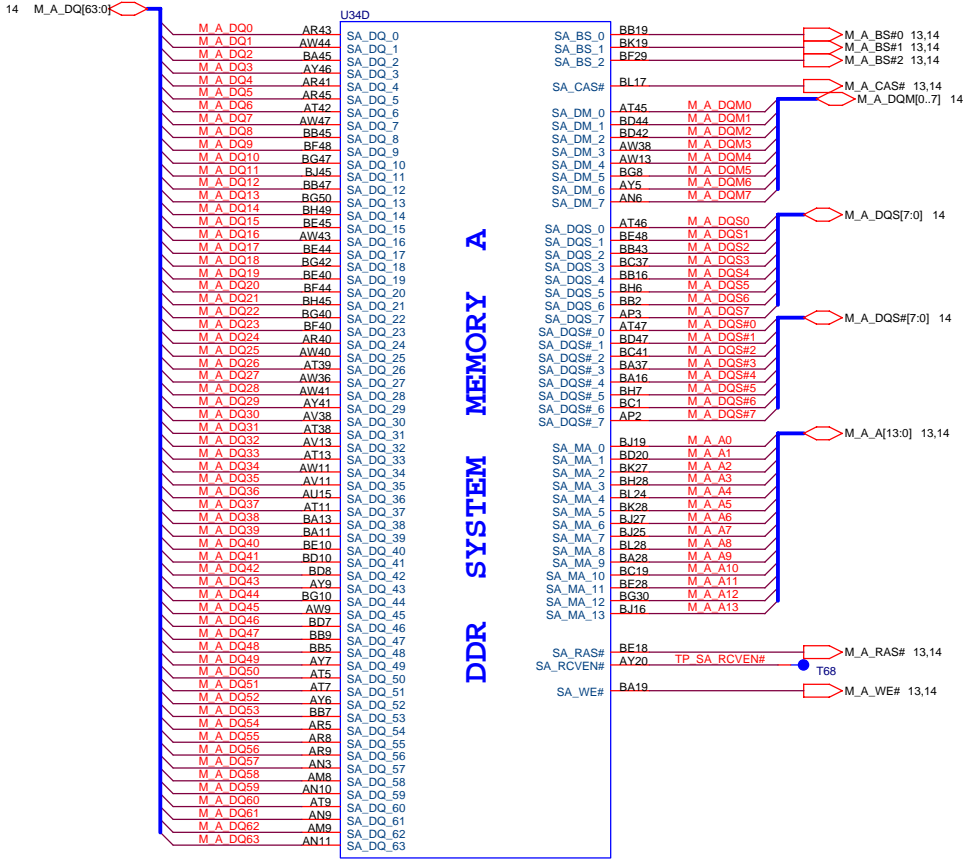
only resever AT375 not  
 support IAGT, but design  
 line suggest to connection  
 these pin , do not NC

CLKREQ# ( MCH drives CLK\_REQ#  
 to control the PCI-E diff clk  
 input itself )

SI-1 modified  
 add 150ohm in  
 the UMA BOM



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Size Custom	Document Number Crestline (DDR)	Rev 1A
Date: Tuesday, January 09, 2007	Sheet 8 of 48	



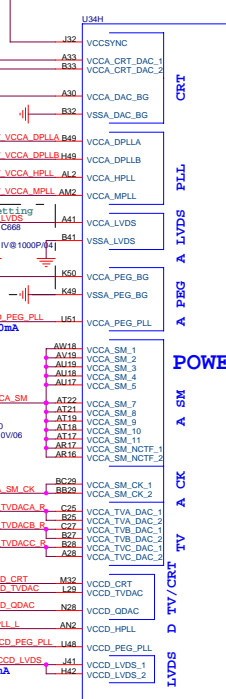
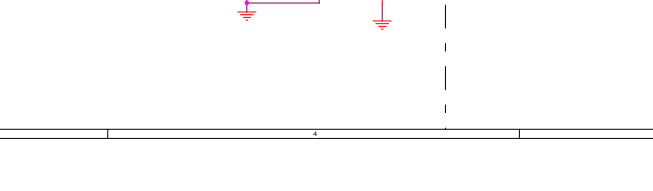
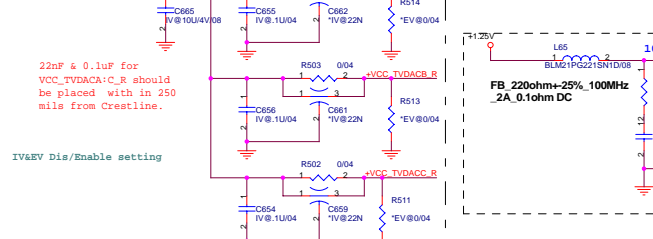
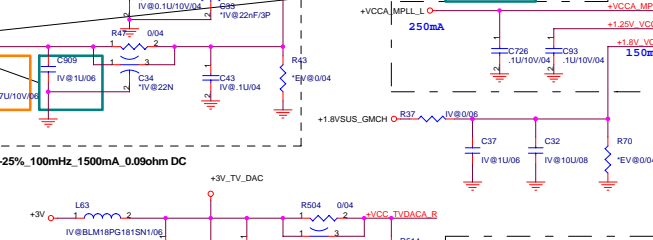
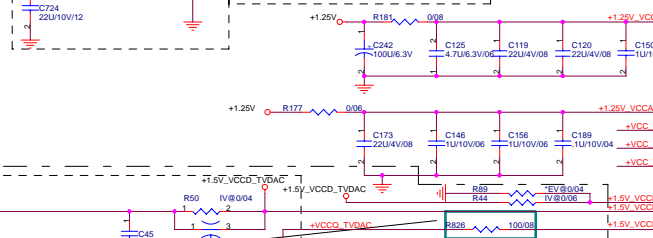
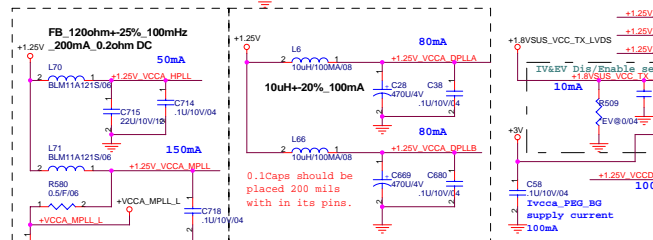
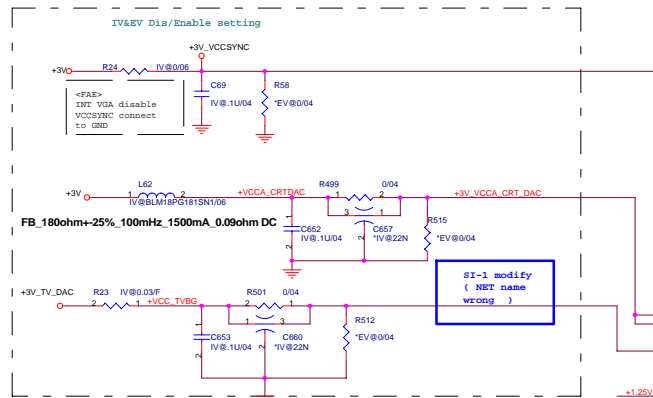


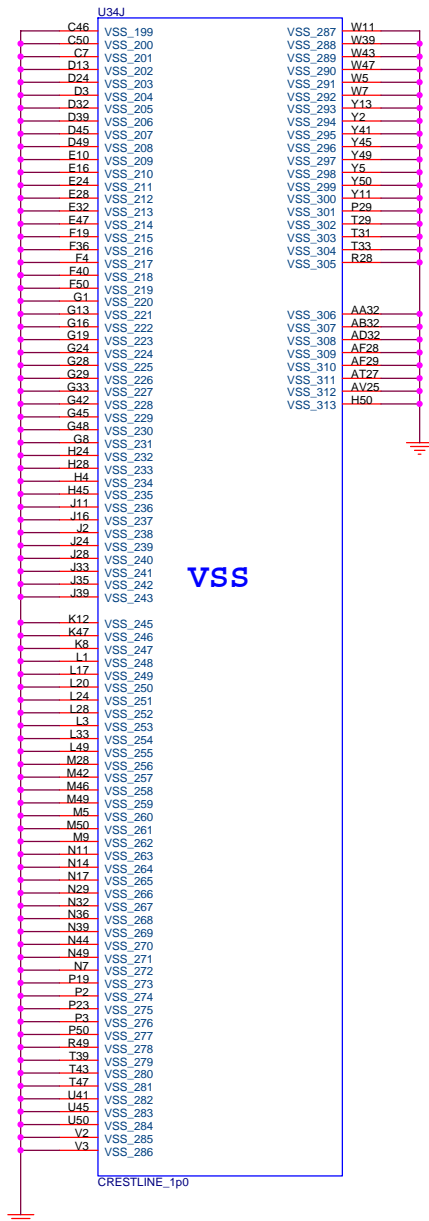
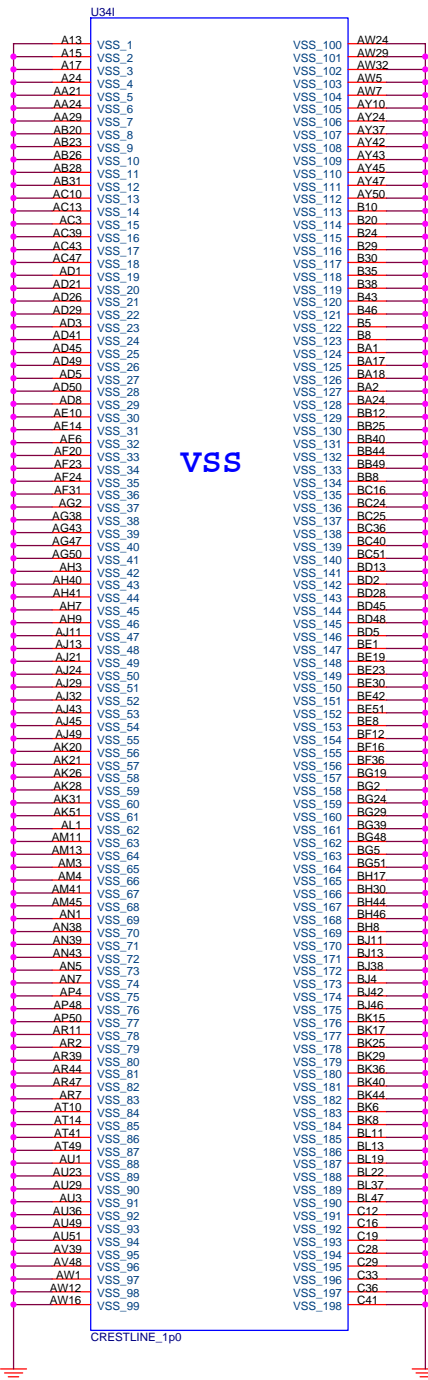

**LVDS Disable/Enable guideline**  
External VGA with SVpart, Internal VGA with IV9 part

Signal	If SDVO Disable LVDS Disable	If LVDS enable
VCCD_LVDS	GND	1.8V
VCCA_LVDS	GND	1.8V
VCCD_TX_LVDS	GND	1.8V

**CRT/TV Disable/Enable guideline**  
External VGA with SVpart, Internal VGA with IV9 part

Ball	Enable	Disable	Ball	Enable	Disable
VCCA_CRT_DAC	3.3V	GND	VCCA_TV_DAC	3.3V	GND
VCCD_CRT	1.5V	GND	VCCD_TV_DAC	1.5V	1.5V
VCCD_QDAC	1.5V	GND	VCCA_DAC_BG	3.3V	GND
VCCA_TV_DAC	3.3V	GND	VSS_DAC_BG	GND	GND
VCCA_TV_DAC	3.3V	GND	VCCSYNC	3.3V	GND



**PROJECT : AT3**  
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Size Custom	Document Number Crestline (VSS)	Rev 1A
Date: Tuesday, January 09, 2007		Sheet 11 of 48

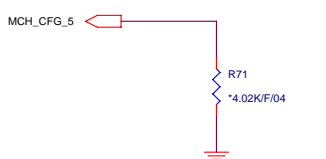
## Strap table

All strap are sampled with respect to the leading edge of the GMCH Power OK(PWROK) Signal  
 CFG[17:3] Have internal Pull-up  
 CFG[18:19] Have internal Pull-down  
 Any CFG signal strapping option not list below should be left NC Pin

Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 = Mobile CPU(Default)
CFG8	Low power PCI Express	0 = Normal mode 1 = Low Power mode
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALLZ	00 = Reserved 01 = XOR Mode Enable 10 = All-Z Mode Enabled 11 = Normal operation(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card present(Default) 1 = SDVO Card Present
CFG19	DMI Lane Reversal	0 = Normal operation(Default) 1 = Reverse Lanes
CFG20	SDVO/PCIE concurrent	0 = Only SDVO or PCIE x1 is operation(Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port

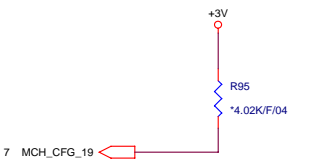
**DMI X2 Select**

MCH_CFG_5	Low = DMIX2 High = IDMIX4(Default)
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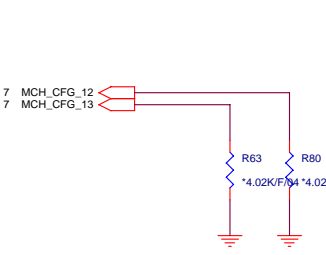
**DMI Lane Reversal**

MCH_CFG_19	Low = Normal operation(Default) High = Reverse Lane
------------	--



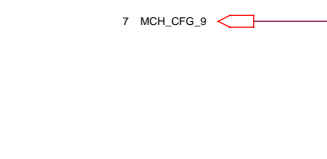
**XOR /ALLZ /Clock Un-gating**

MCH_CFG_12	MCH_CFG_13	Configuration
0	0	Clock gating disable
0	1	XOR Mode Enable
1	0	ALL-z Mode Enable
1	1	Normal operation(Default)



**PCI Express Graphics**

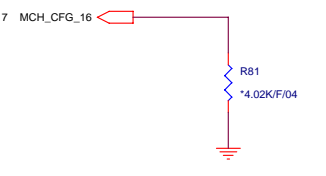
MCH_CFG_9	Low = Reverse Lane High = Normal operation(Default)
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**SDVO Present**  
 Strap define at External DVI control page

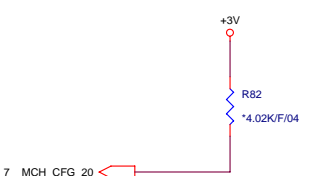
**FSB Dynamic ODT**

MCH_CFG_16	Low = ODT Disable High = ODT Enable(Default)
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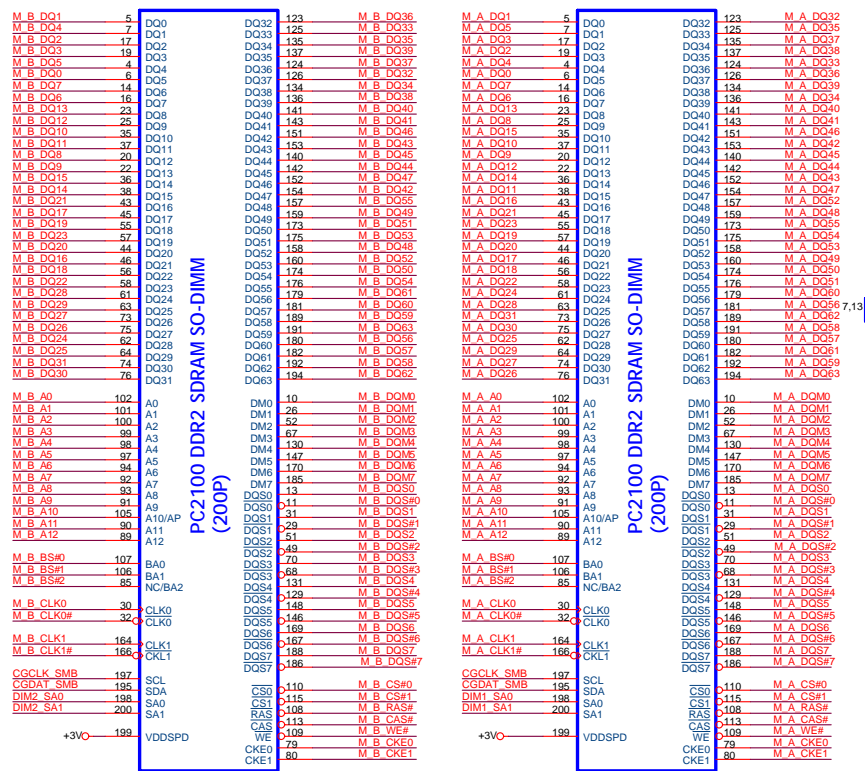
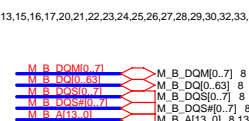
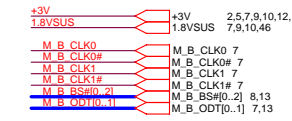
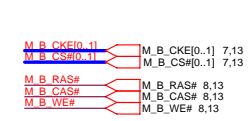
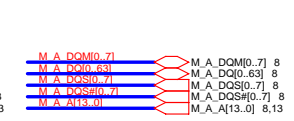
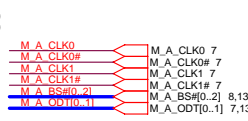
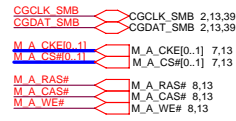
**SDVO/PCIE Concurrent operation**

MCH_CFG_20	Low = Only SDVO or PCIE X1 is operational(Default) High = SDVO and PCIE X1 are operating simultaneously via the PEG port
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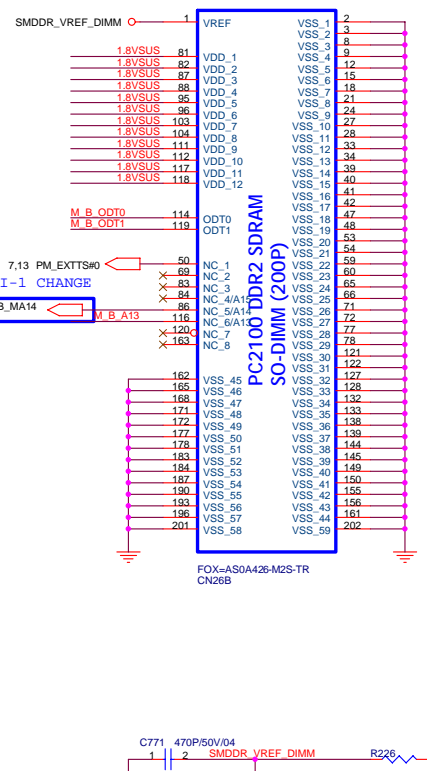
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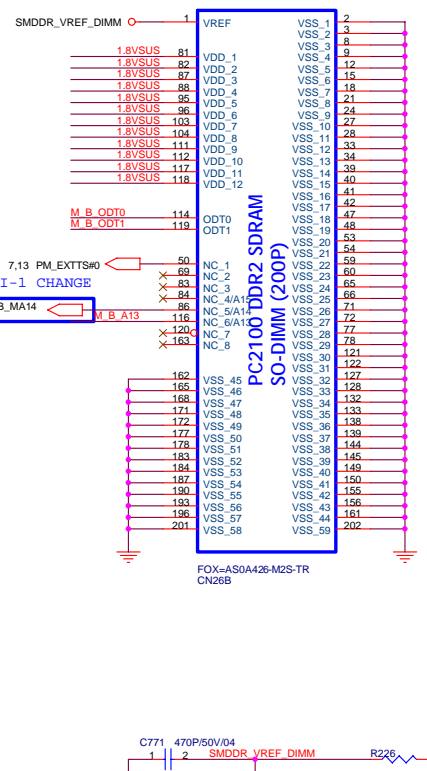
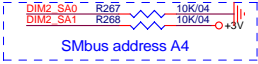
CKEA,0,1

CKEB,0,1

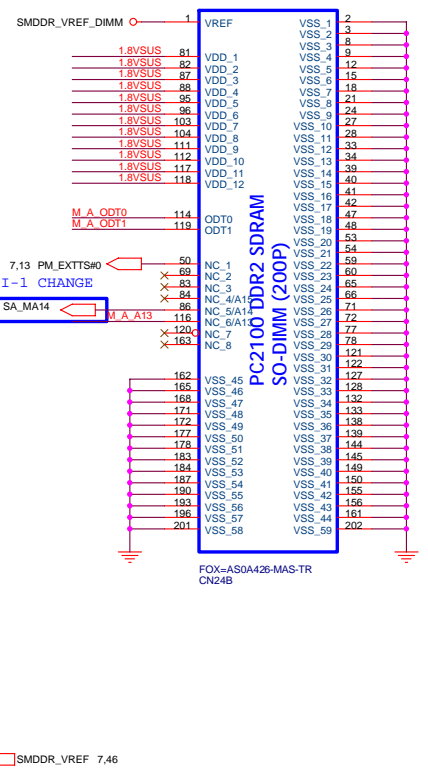


H 9.2

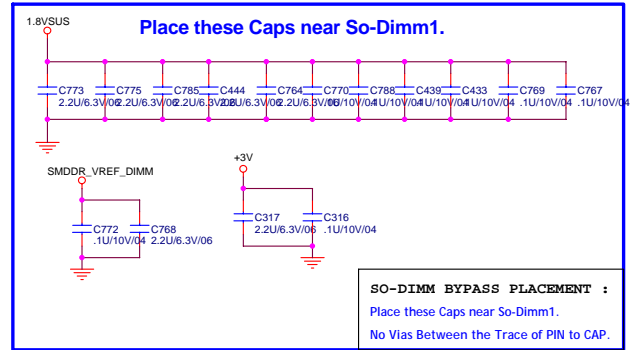
H 5.2



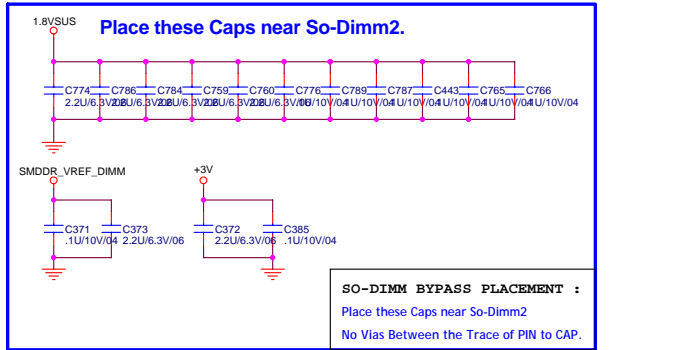
FOX=AS0A426-M2S-TR CN26B



FOX=AS0A426-MAS-TR CN24B



SO-DIMM BYPASS PLACEMENT : Place these Caps near So-Dimm1. No Vias Between the Trace of PIN to CAP.



SO-DIMM BYPASS PLACEMENT : Place these Caps near So-Dimm2. No Vias Between the Trace of PIN to CAP.



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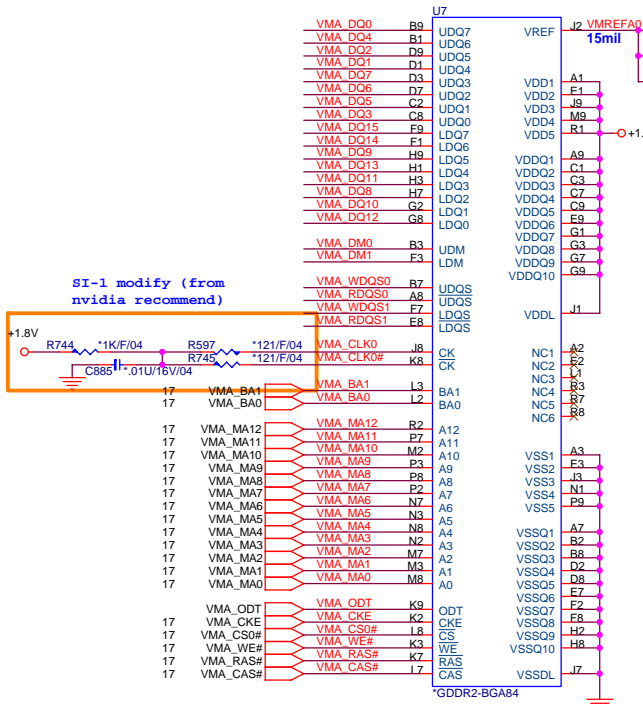
Table with columns: Size Custom, Document Number, Rev. Content: DDRII SO-DIMM(200P), Rev 1A, Date: Tuesday, January 09, 2007, Sheet 14 of 48



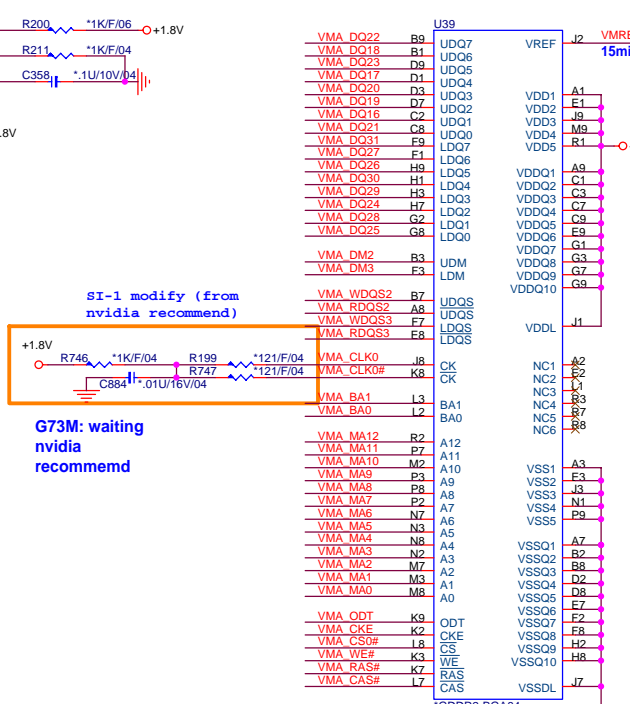






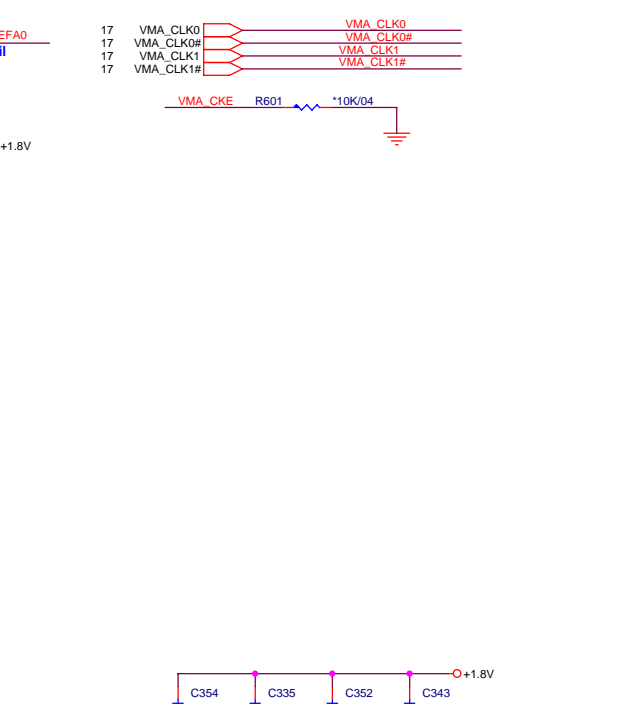


SI-1 modify (from nvidia recommend)

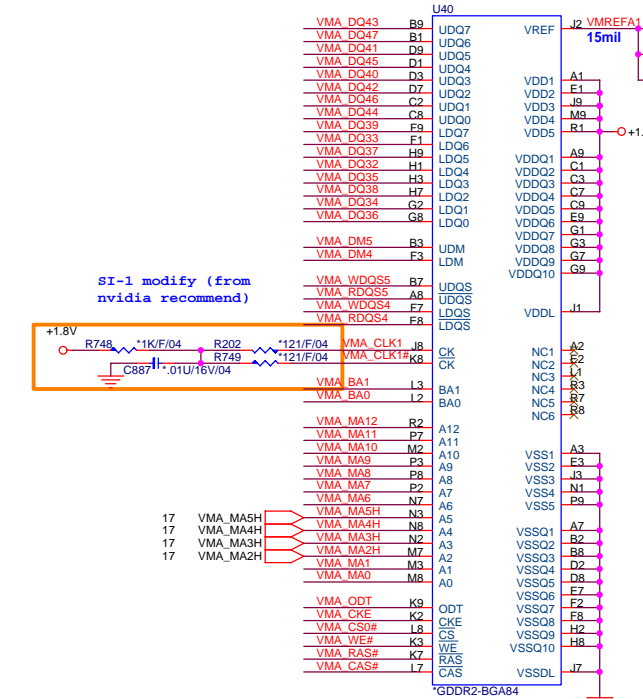


SI-1 modify (from nvidia recommend)

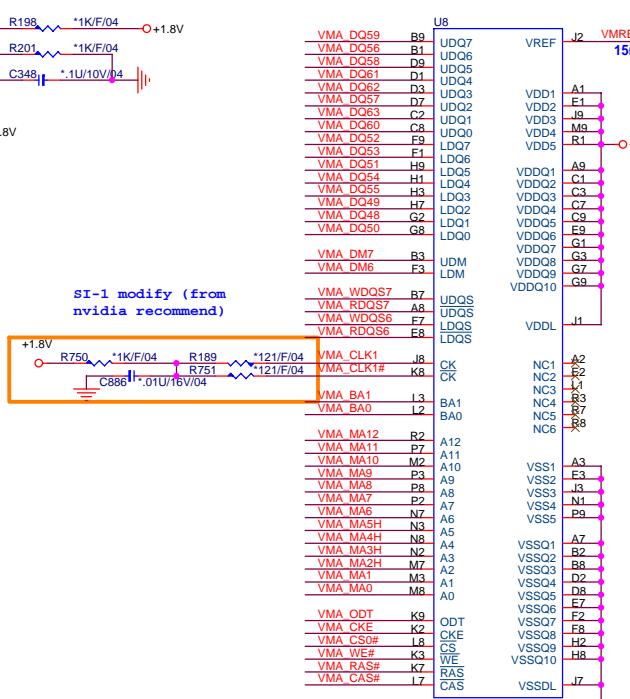
G73M: waiting nvidia recommend



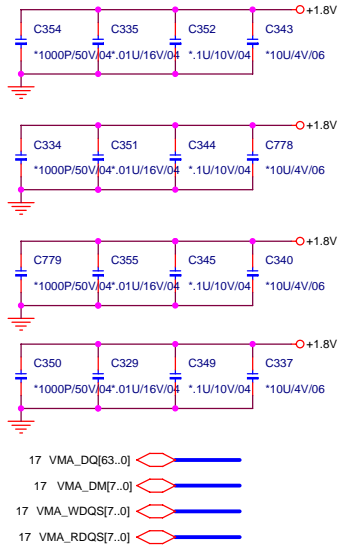
256Mb : AKD5JGAT\*05  
512Mb : AKD59G-T\*01



SI-1 modify (from nvidia recommend)

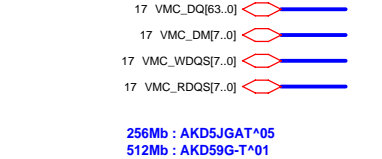
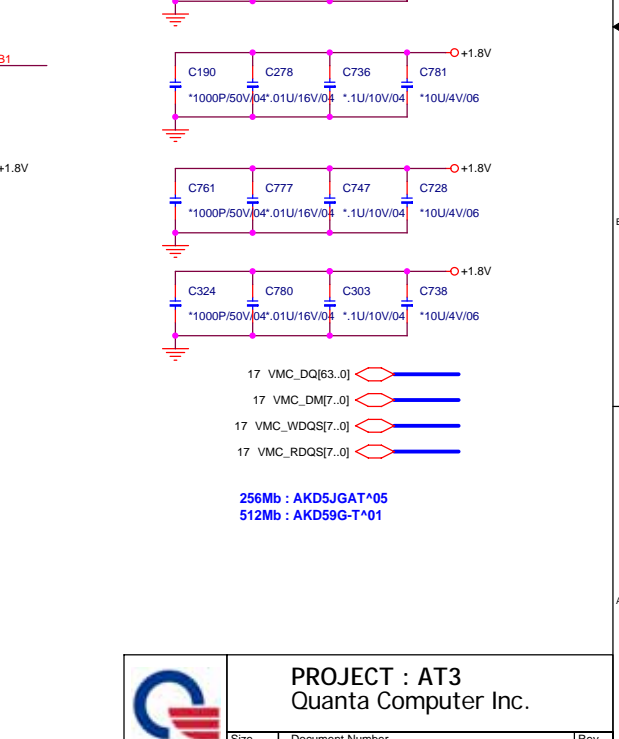
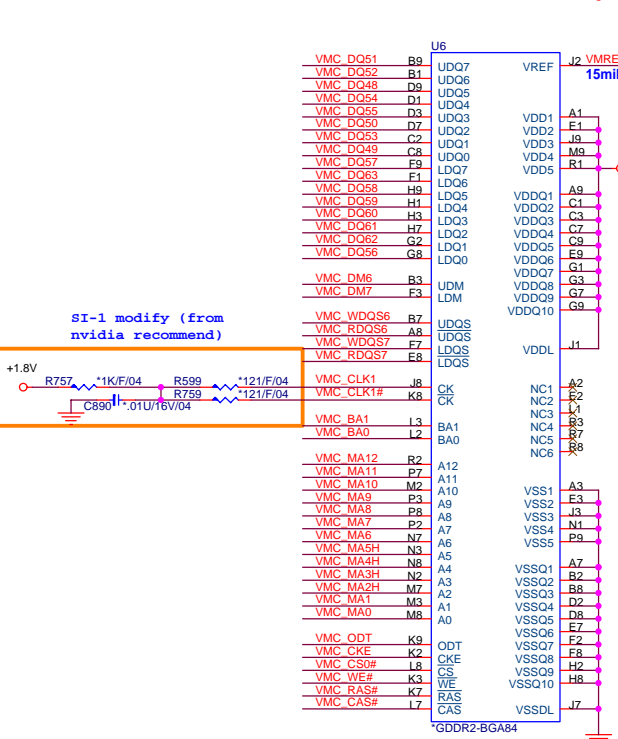
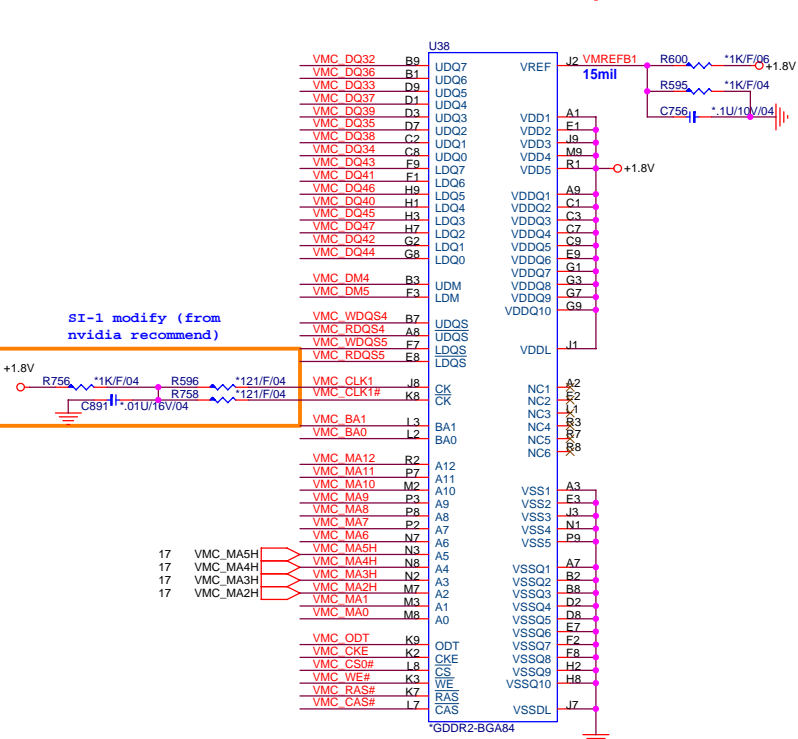
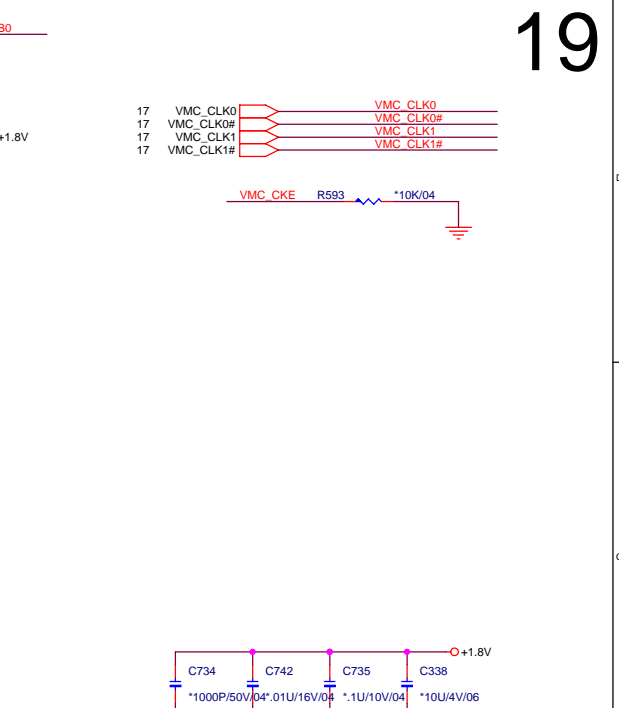
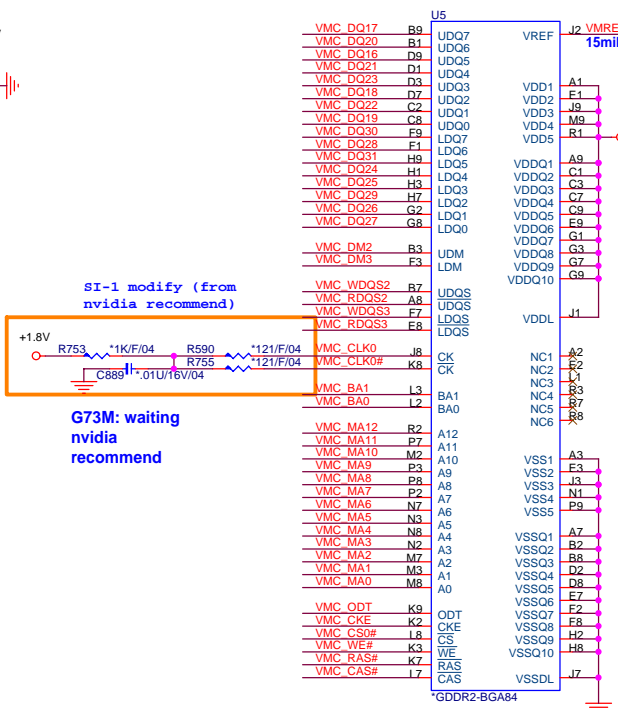
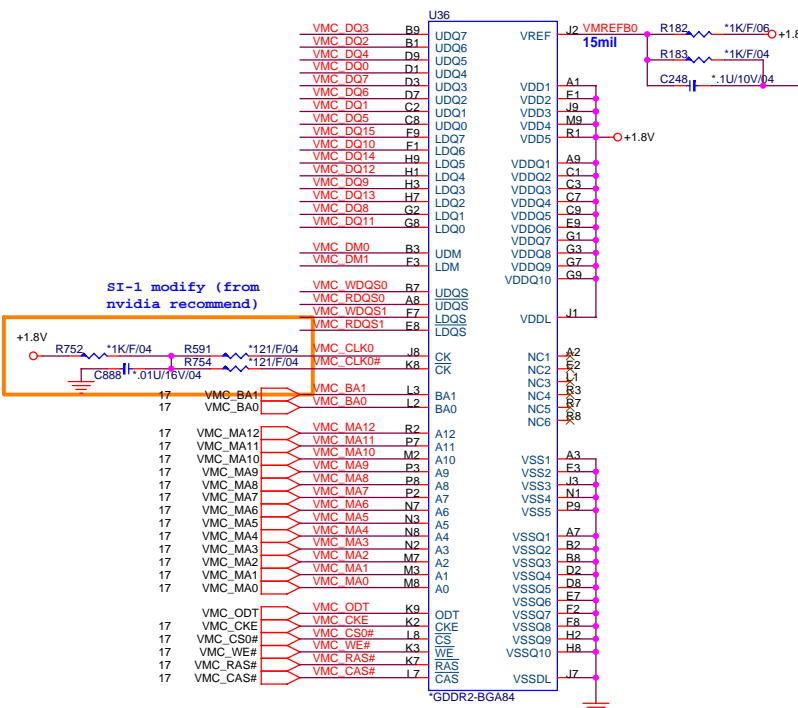


SI-1 modify (from nvidia recommend)



PROJECT : AT3  
Quanta Computer Inc.

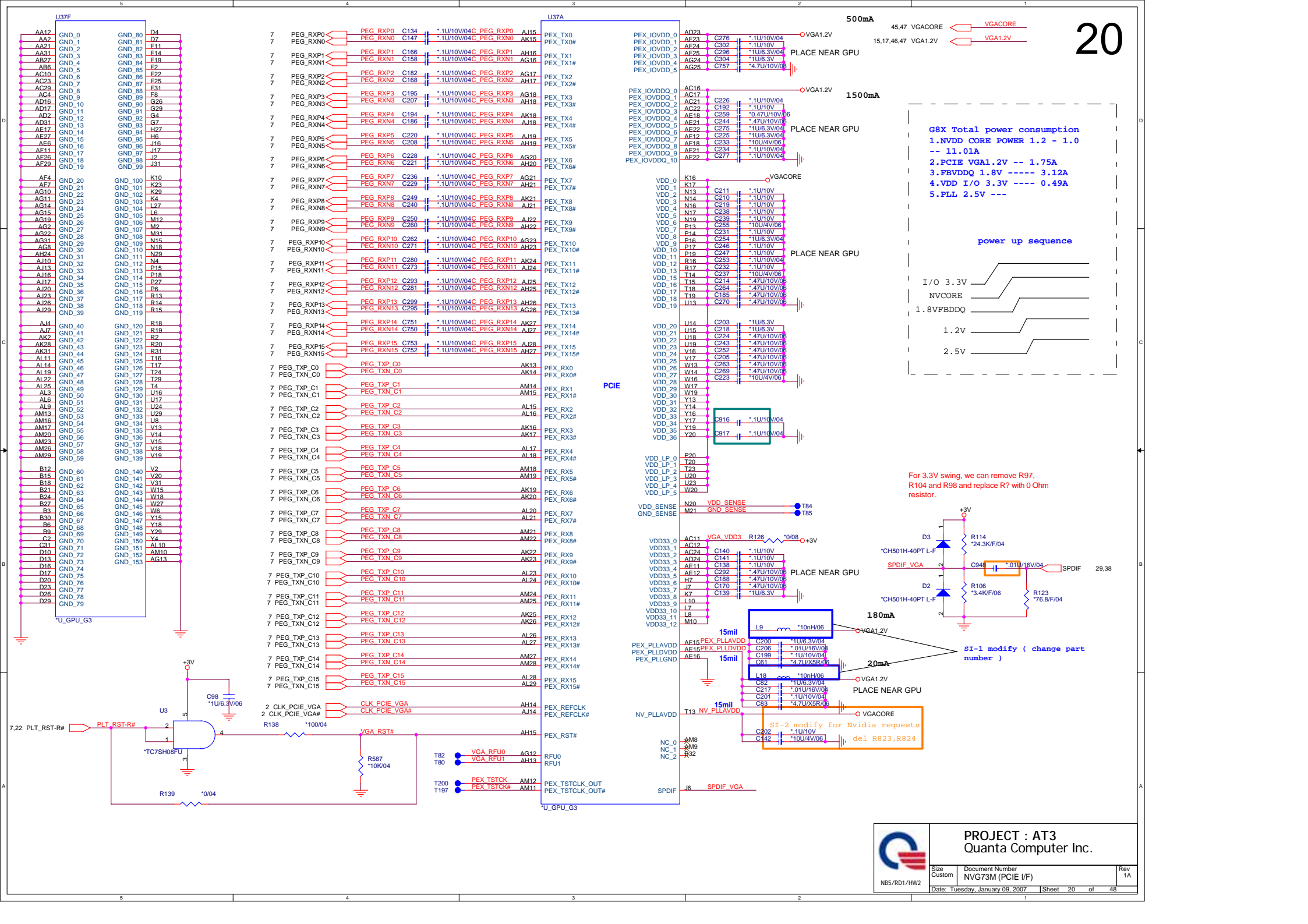
Size Custom	Document Number NVG73M V-RAN-1(GDDR2 BGA84)	Rev 1A
Date: Tuesday, January 09, 2007		Sheet 18 of 48



256Mb : AKD5JGAT\*05  
512Mb : AKD59G-T\*01

**PROJECT : AT3**  
**Quanta Computer Inc.**

Size Custom	Document Number NVG73M VREM-2(GDDR2 BGA84)	Rev 1A
Date: Tuesday, January 09, 2007   Sheet 19 of 48		



500mA 45.47 VGACORE  
15.17,46,47 VGA1.2V

1500mA  
PLACE NEAR GPU

PLACE NEAR GPU

PLACE NEAR GPU

PLACE NEAR GPU

PLACE NEAR GPU

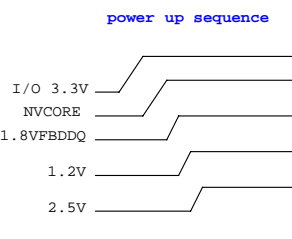
PLACE NEAR GPU

PLACE NEAR GPU

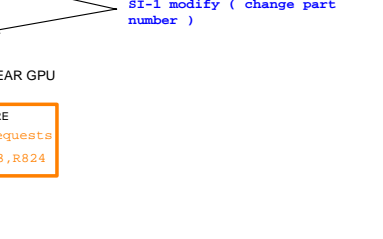
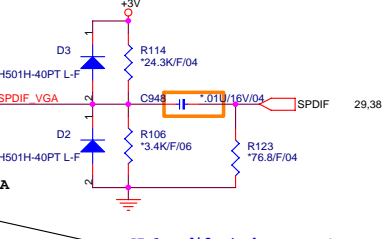
PLACE NEAR GPU

PLACE NEAR GPU

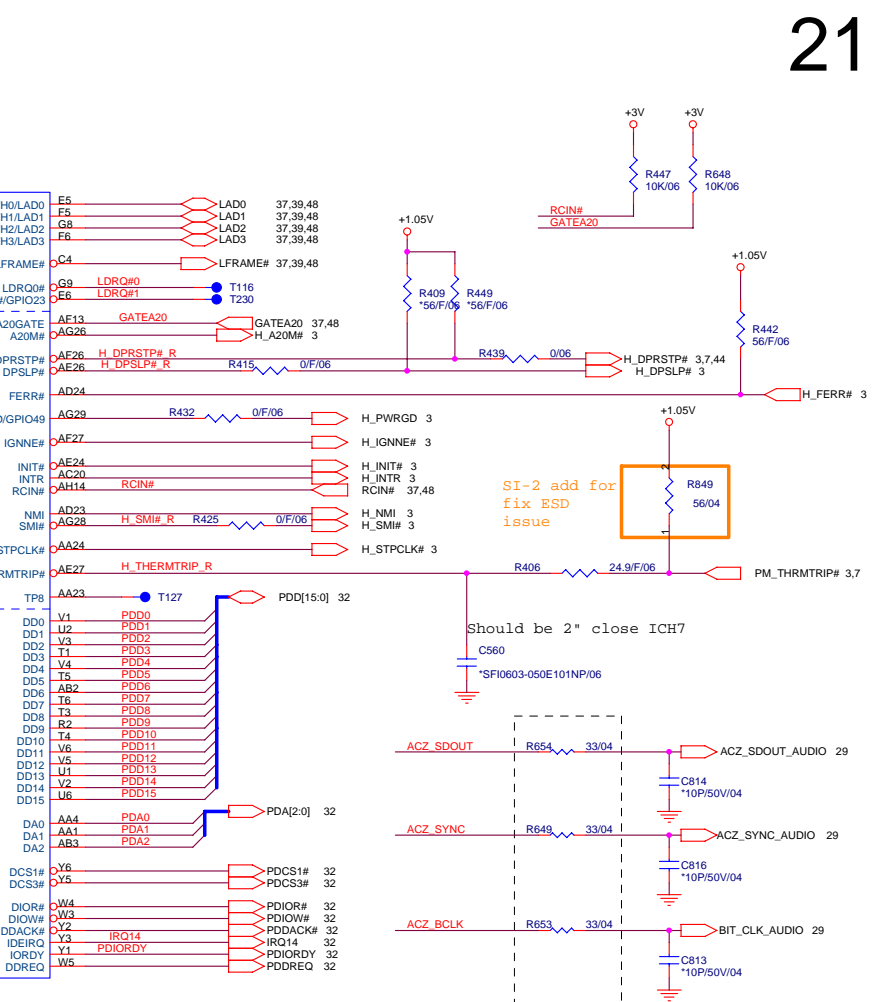
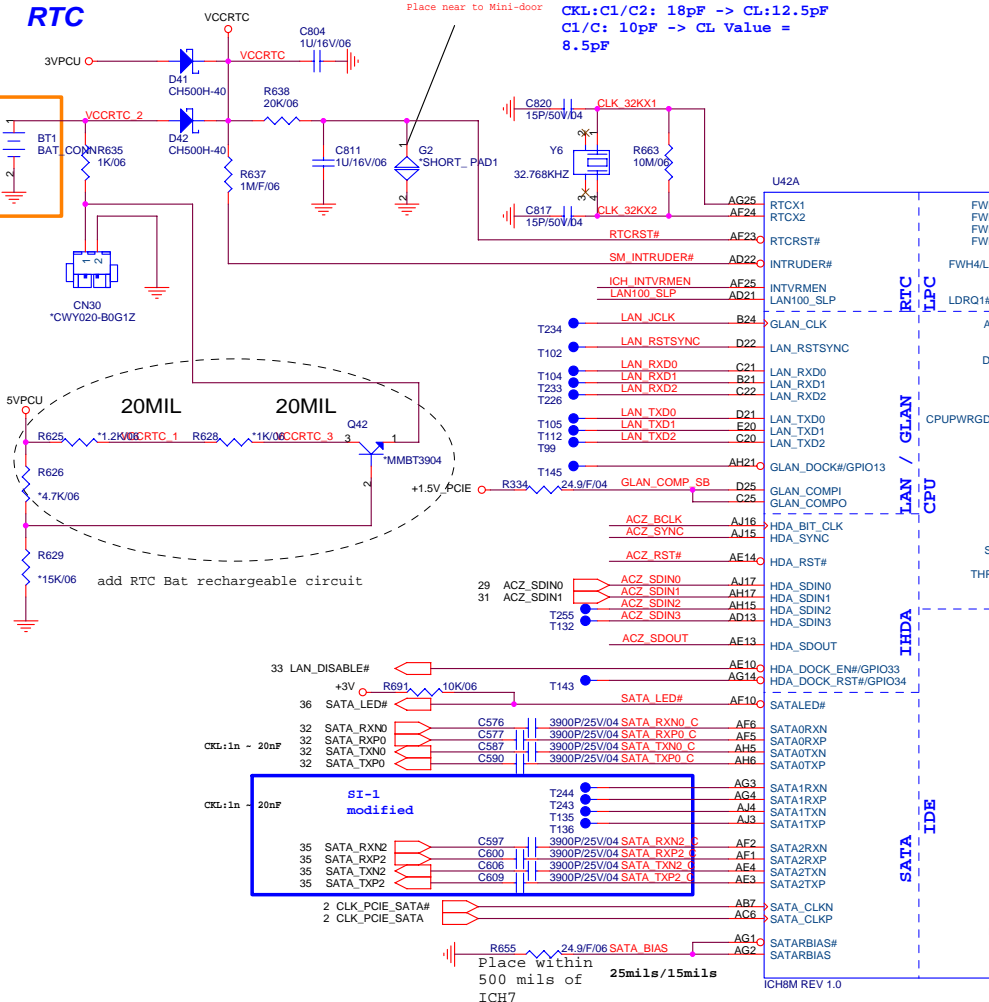
- G8X Total power consumption
- 1.NVDD CORE POWER 1.2 - 1.0 -- 11.01A
- 2.PCIE VGA1.2V -- 1.75A
- 3.FBDDQ 1.8V ----- 3.12A
- 4.VDD I/O 3.3V ----- 0.49A
- 5.PLL 2.5V ---



For 3.3V swing, we can remove R97, R104 and R98 and replace R7 with 0 Ohm resistor.



**RTC**



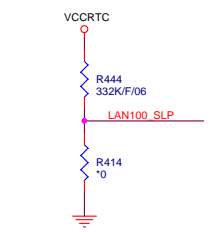
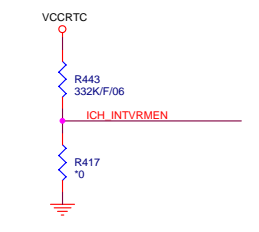
**SB Strap**

**ICH8-M Internal VR Enable strap**  
(Internal VR for Vccsus1\_05, VccSus1\_5 and VccCL1\_5)

INTVRMEN	Low = Internal VR disable High = Internal VR enable(Default)
----------	---

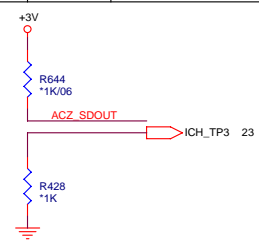
**ICH8-M LAN100\_SLP Strap**  
(Internal VR for VccLAN1\_05 and VccCL1\_05)

LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)
------------	---

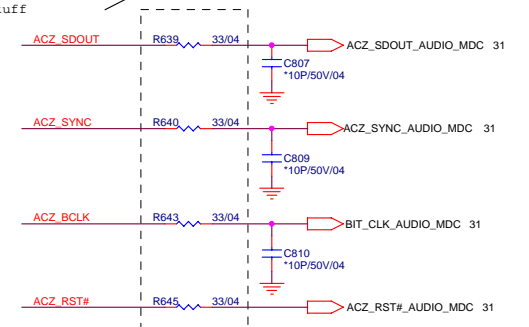


**XOR Chain Entrance Strap**

ICH_RSVO	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal operation(Default)
1	1	Set PCIE port config bit 1

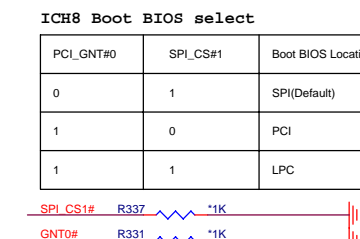
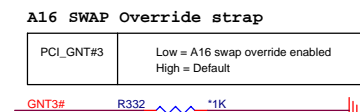
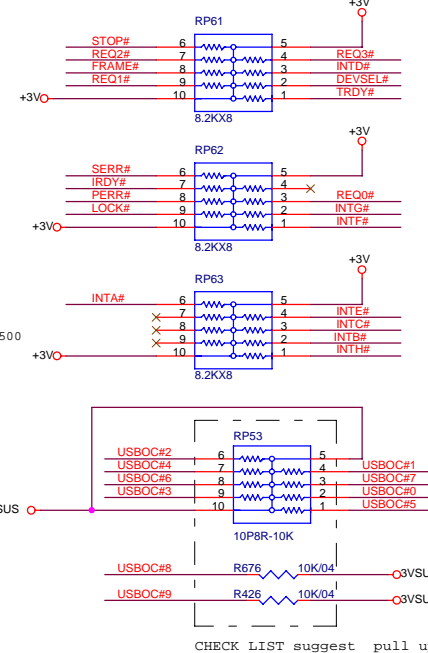
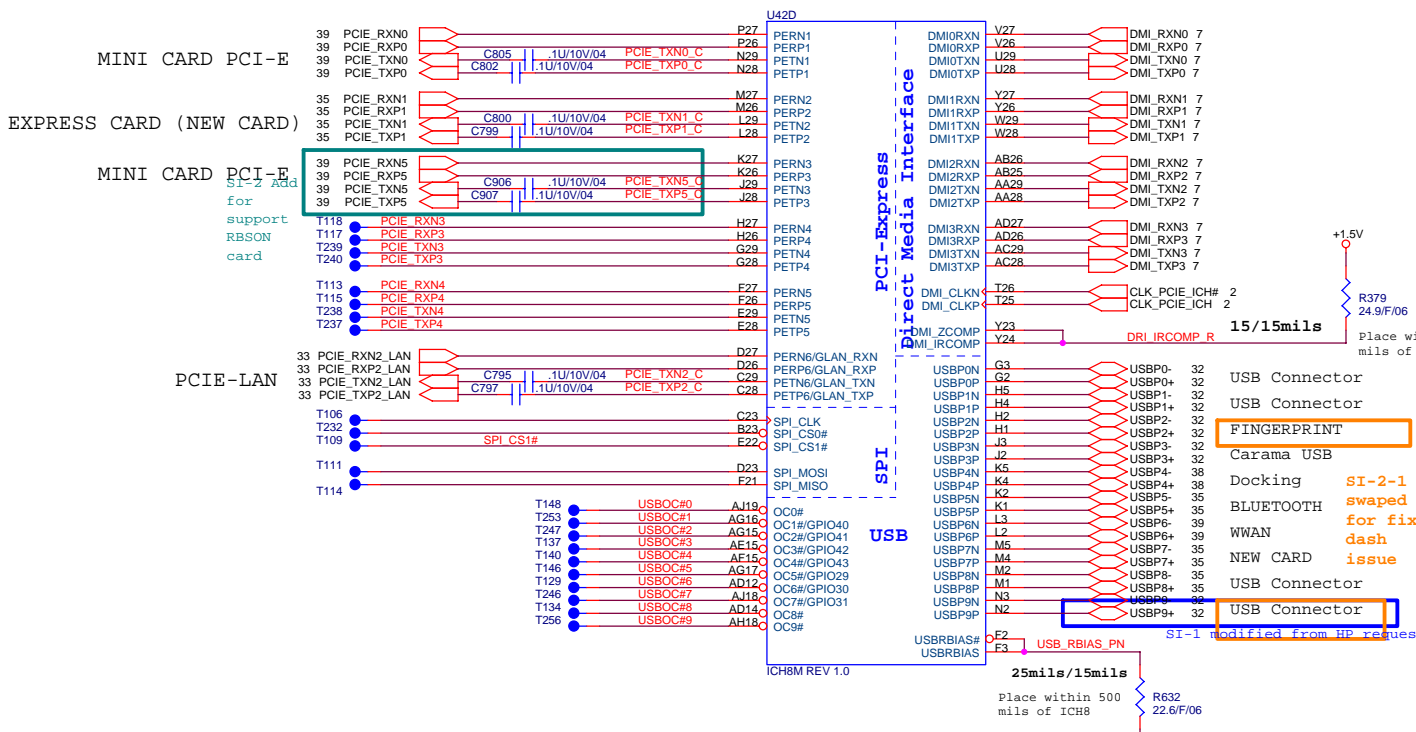


intel check list  
define to stuff  
33ohm



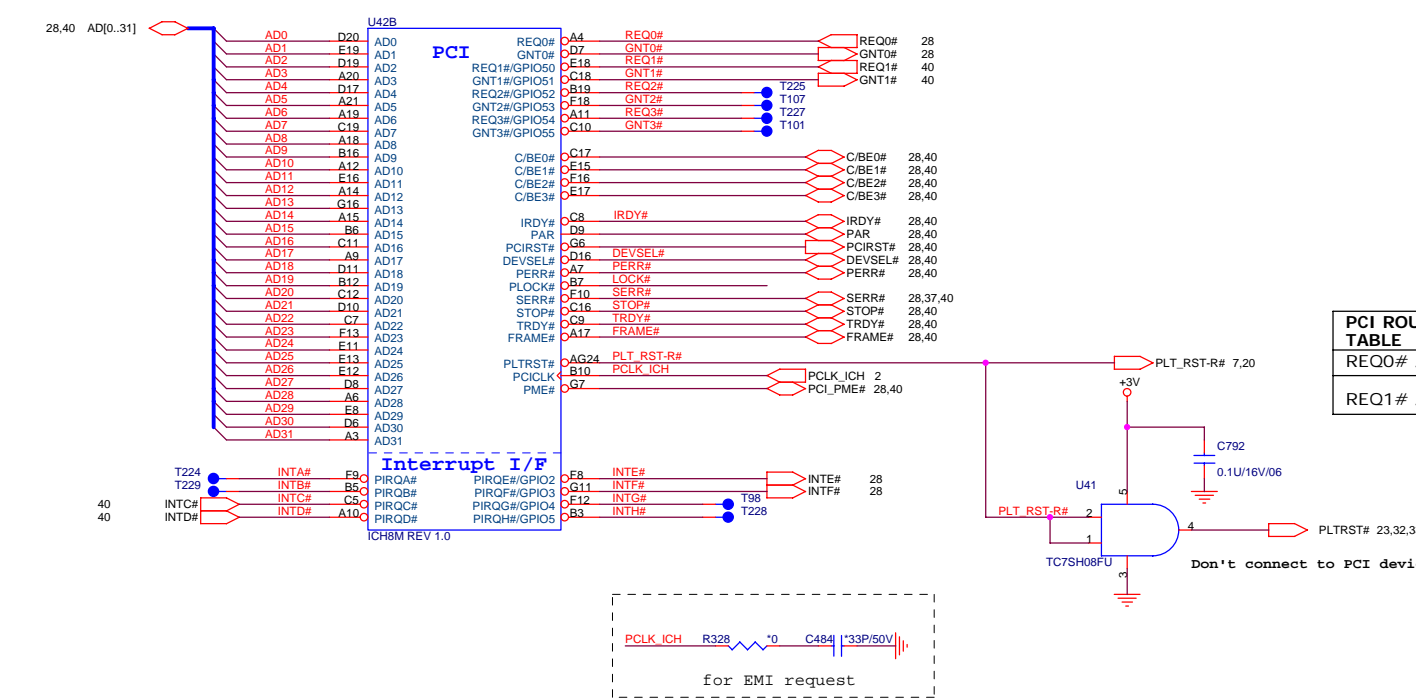
**PROJECT : AT3**  
Quanta Computer Inc.

Size Custom	Document Number ICH7-M HOST(1/4)	Rev 1A
Date: Tuesday, January 09, 2007		Sheet 21 of 48



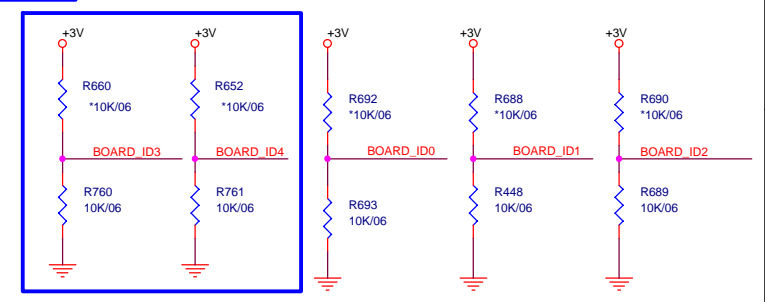
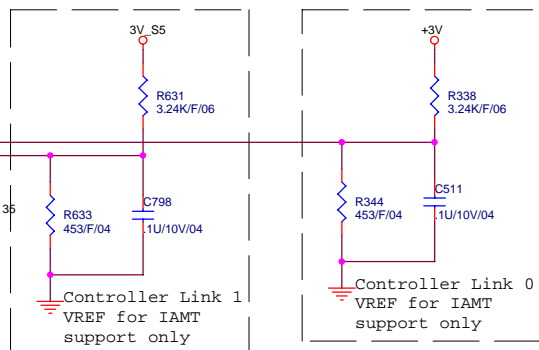
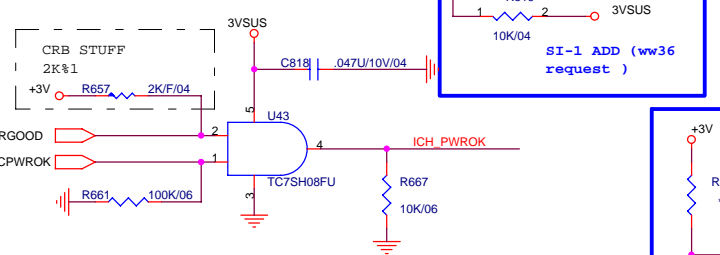
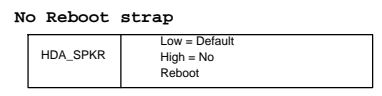
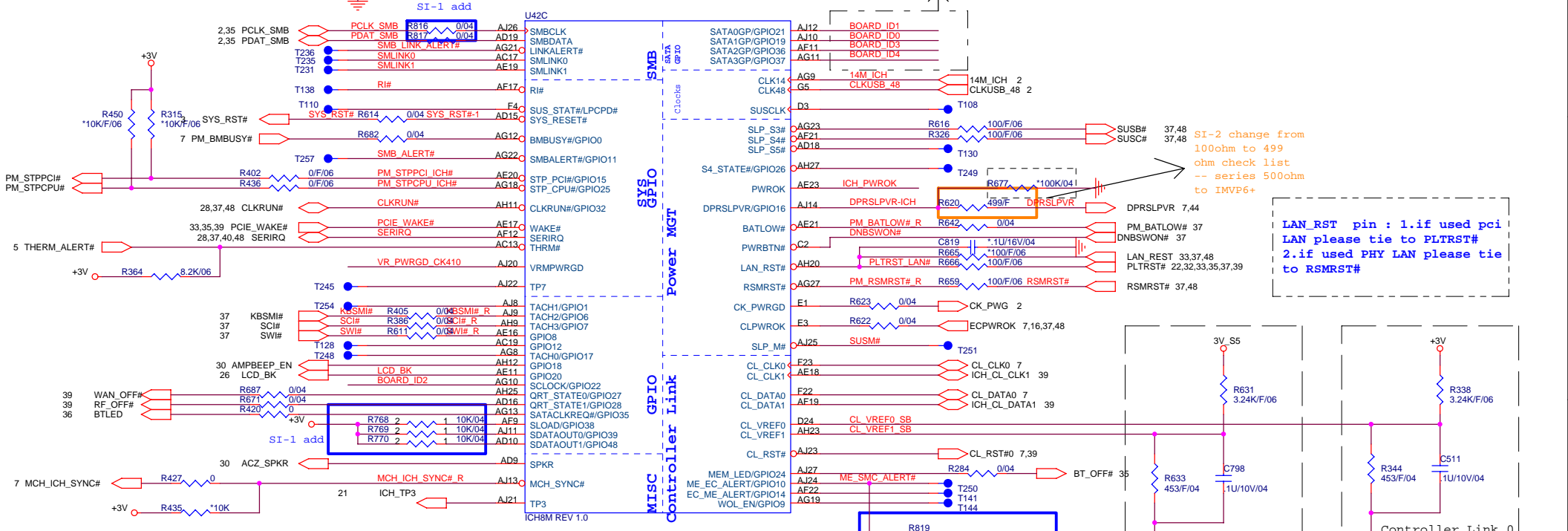
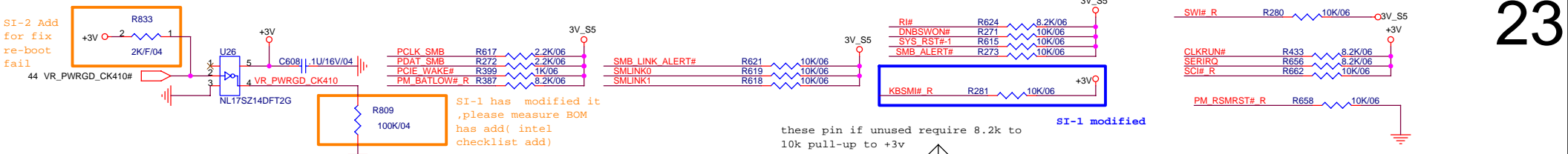
**PCI ROUTING TABLE**

REQ# / GNT0#	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD25	INTE#,INTF#	RICOH832
REQ1# / GNT1#	AD22	INTC#,INTD#	MINI PCI for debug

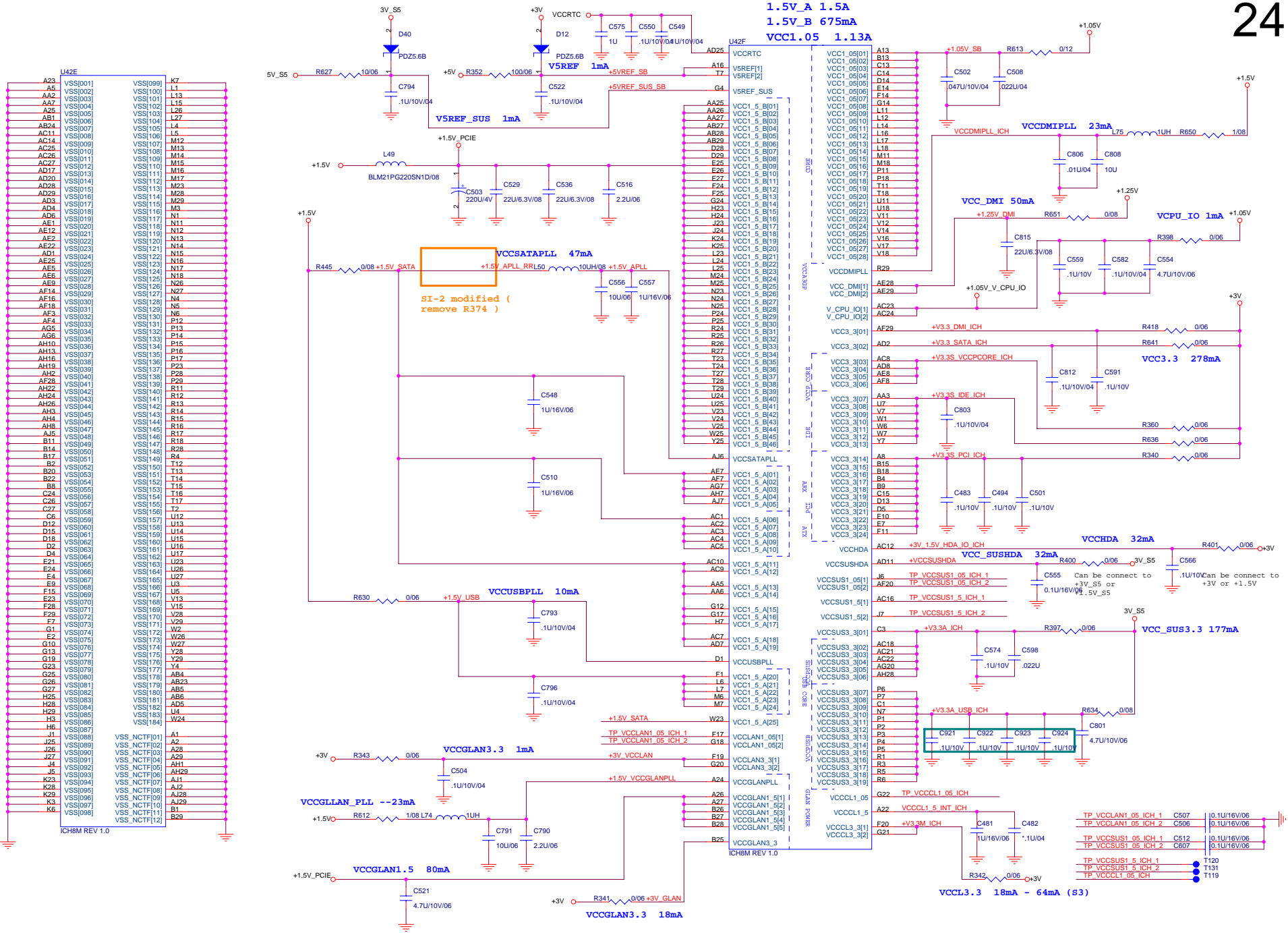


**PROJECT : AT3**  
 Quanta Computer Inc.

Size Custom | Document Number ICH7-M M PCI E(2/4) | Rev 1A  
 Date: Tuesday, January 09, 2007 | Sheet 22 of 48



Board ID	15 " PAV UMA 965GM	15" PRE UMA 965GM	15"PAV Discrete 965PM+G86MV+128M	17" PAV Discrete 965PM+G86MV+128M	17" PAV Discrete 965PM+G84MV+256M	17" PAV UMA 965GM
	(0:0:0)	(0:0:1)	(0:1:0)	(0:1:1)	(1:0:0)	(1:0:1)
ID0	R693 Stuff	R692 Stuff	R693 Stuff	R692 Stuff	R693 Stuff	R692 Stuff
ID1	R448 Stuff	R448 Stuff	R688 Stuff	R688 Stuff	R448 Stuff	R448 Stuff
ID2	R689 Stuff	R689 Stuff	R689 Stuff	R689 Stuff	R690 Stuff	R690 Stuff

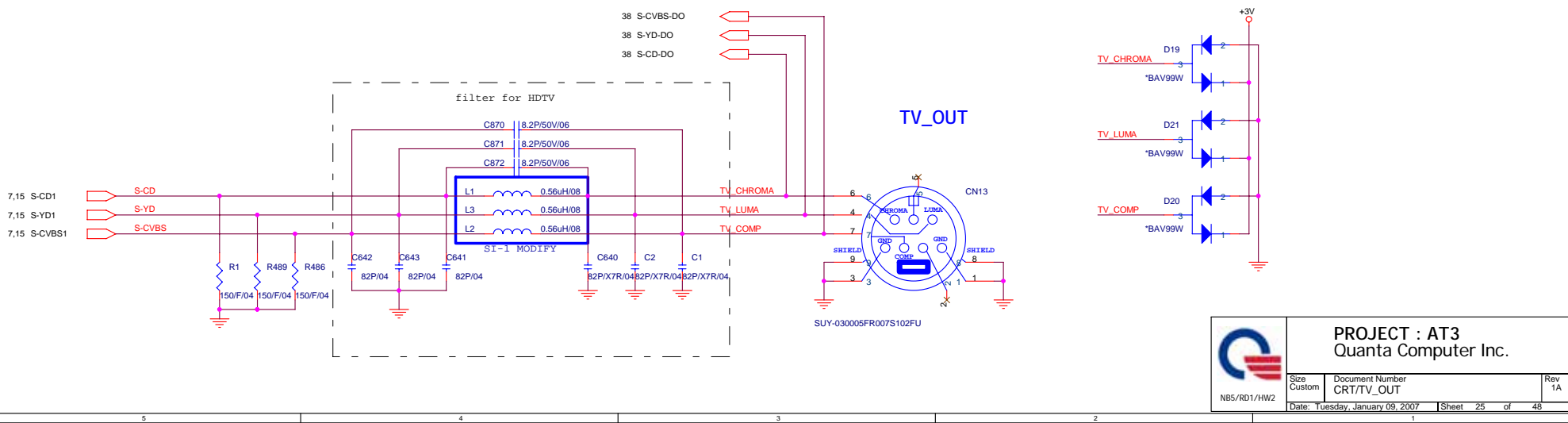
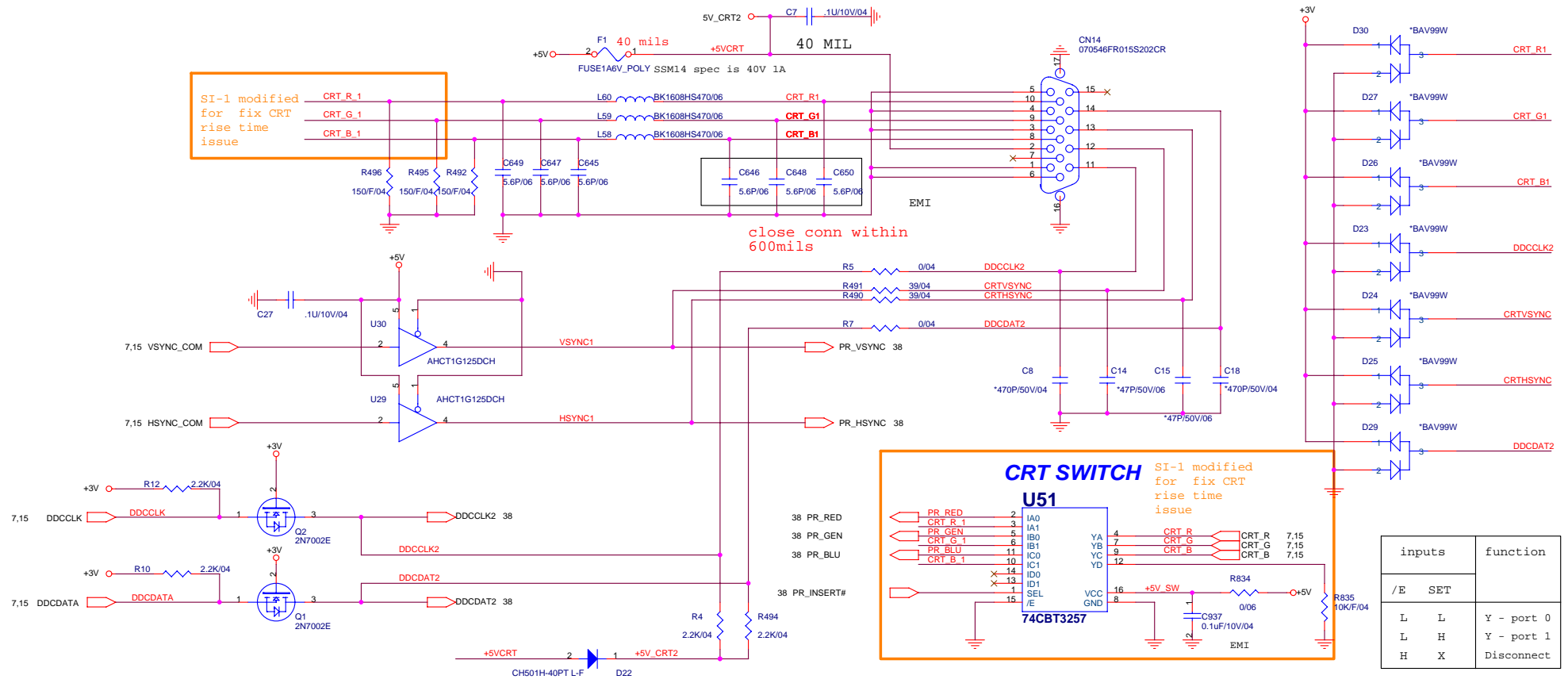


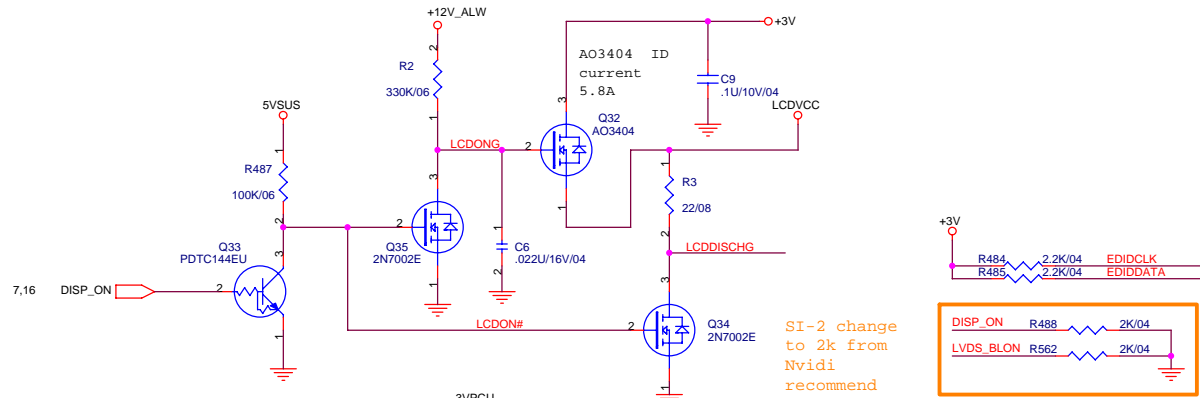
**PROJECT : AT3**  
Quanta Computer Inc.

Size Custom	Document Number ICH7-M POWER(4/4)	Rev 1A
Date: Tuesday, January 09, 2007		Sheet 24 of 48

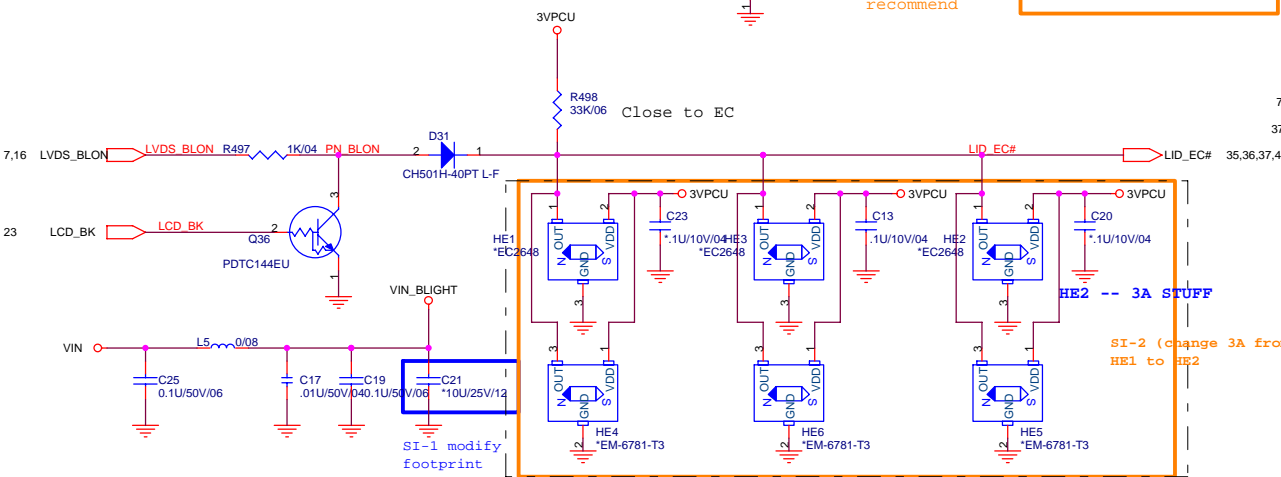
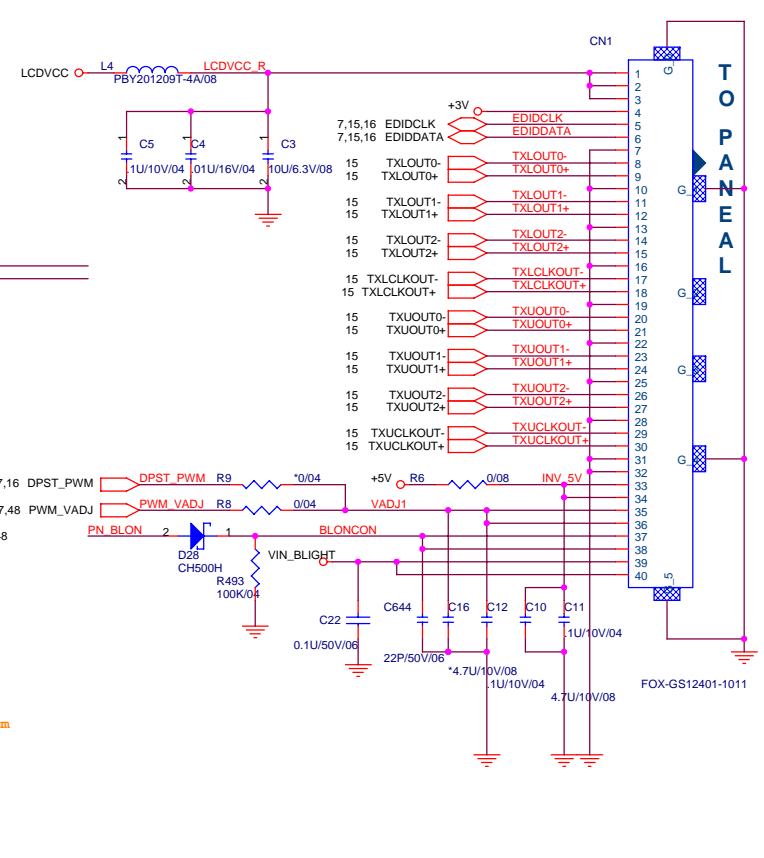


CRT PORT

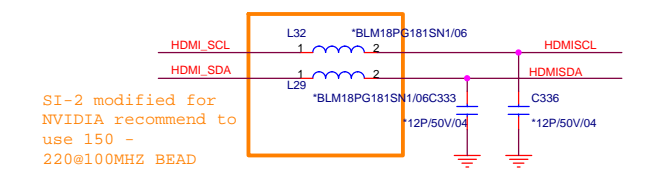




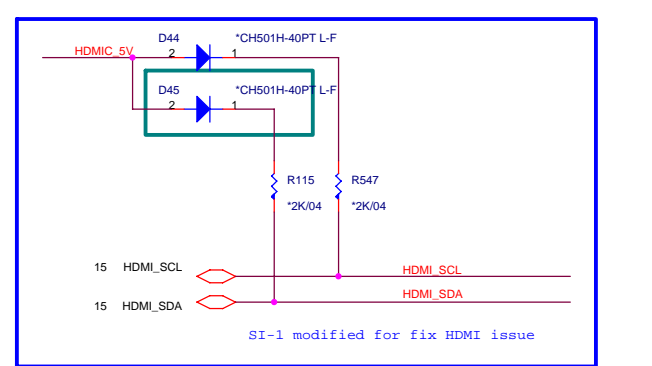
SI-2 change to 2k from Nvidia recommend



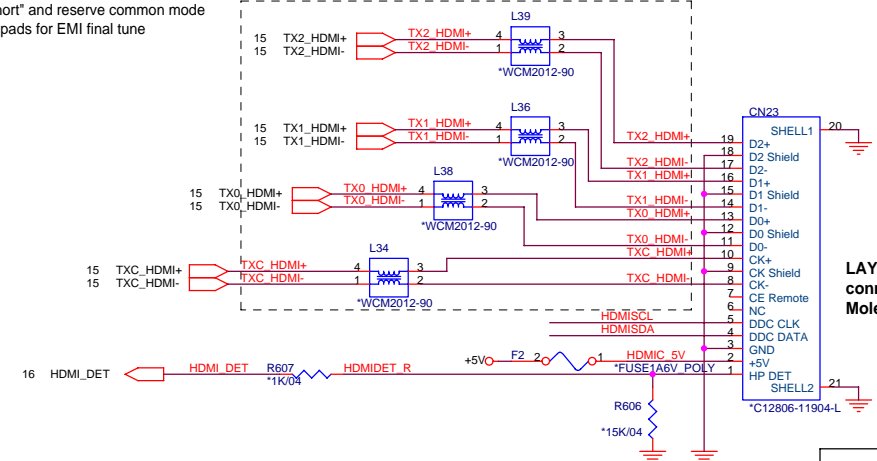
SI-1 modify footprint



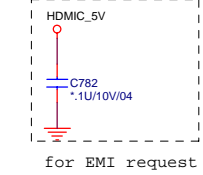
DB "short" and reserve common mode choke pads for EMI final tune



SI-1 modified for fix HDMI issue



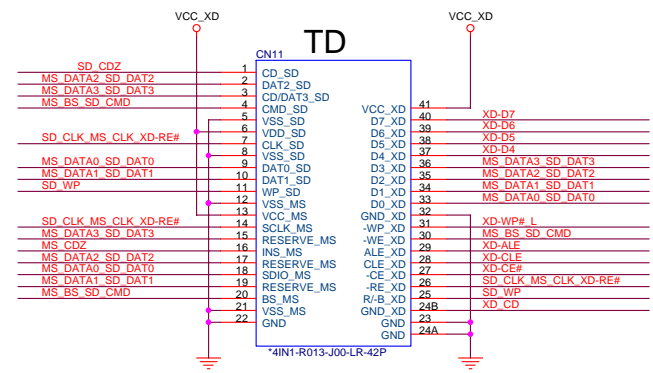
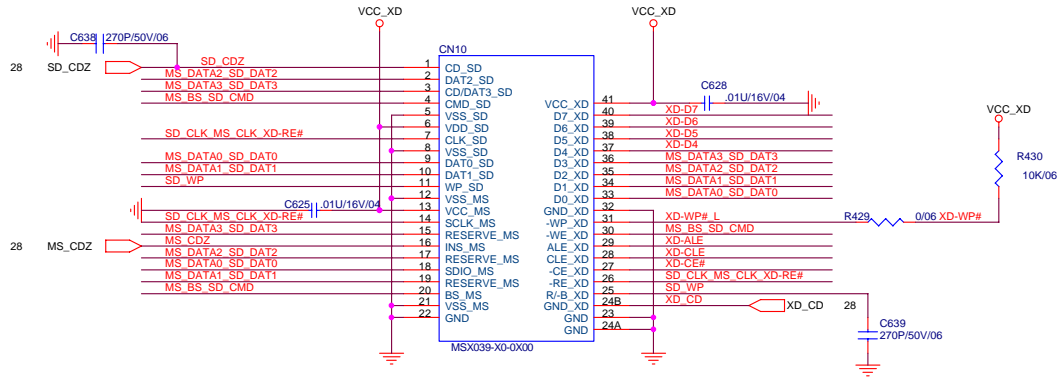
## HDMI PORT



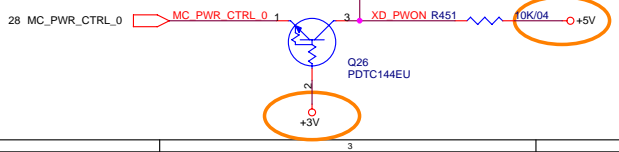
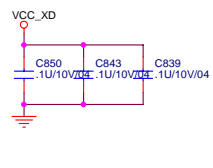
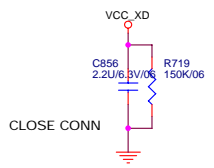
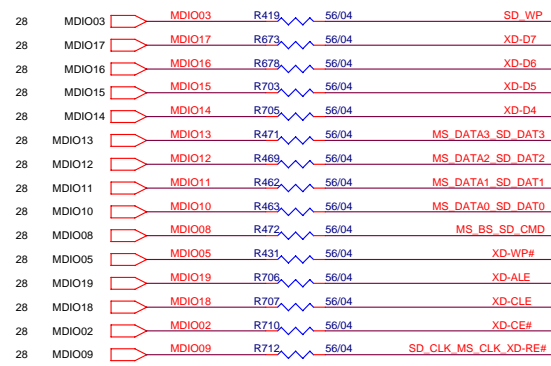
**PROJECT : AT3**  
Quanta Computer Inc.

Size Custom	Document Number LCD CONN/HDMI CONN	Rev 1A
Date: Tuesday, January 09, 2007	Sheet 26 of 48	

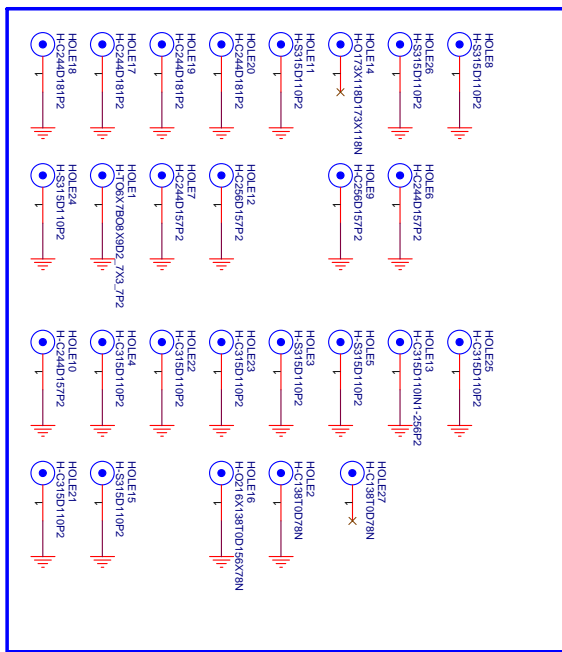
## 5 IN1 CARD READER XD, MMC/SD, MS/MSP



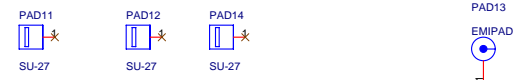
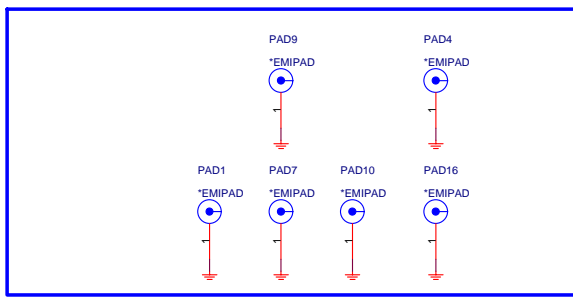
bom create 2'nd source



## SCREW HOLE



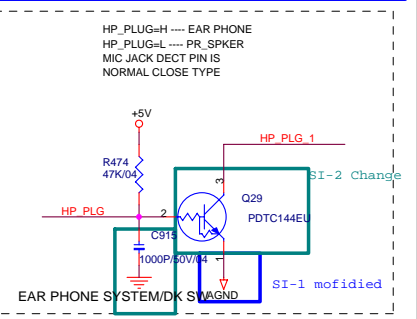
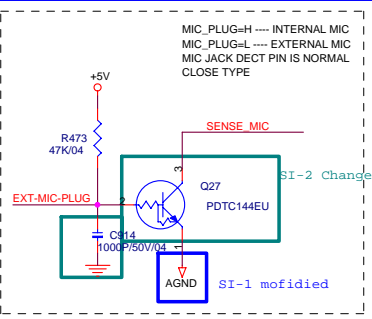
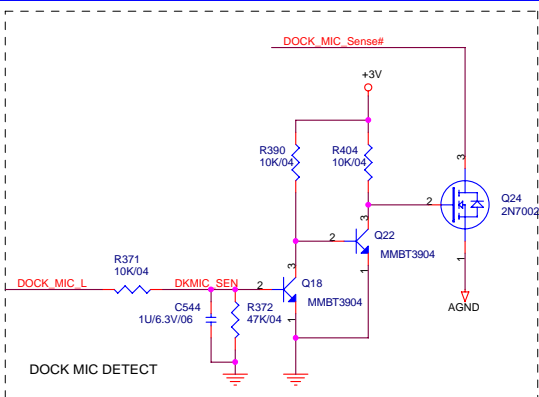
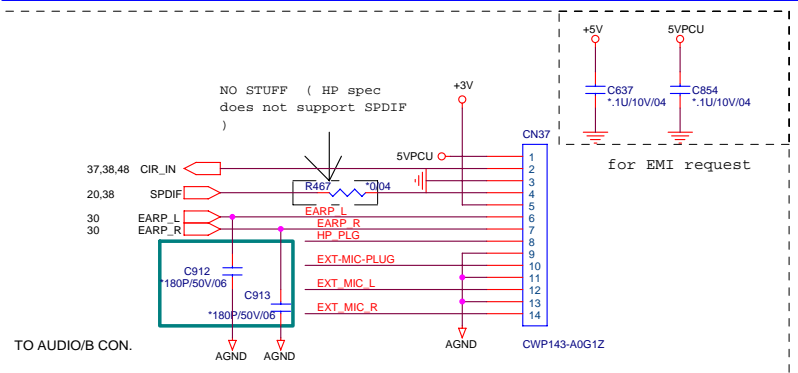
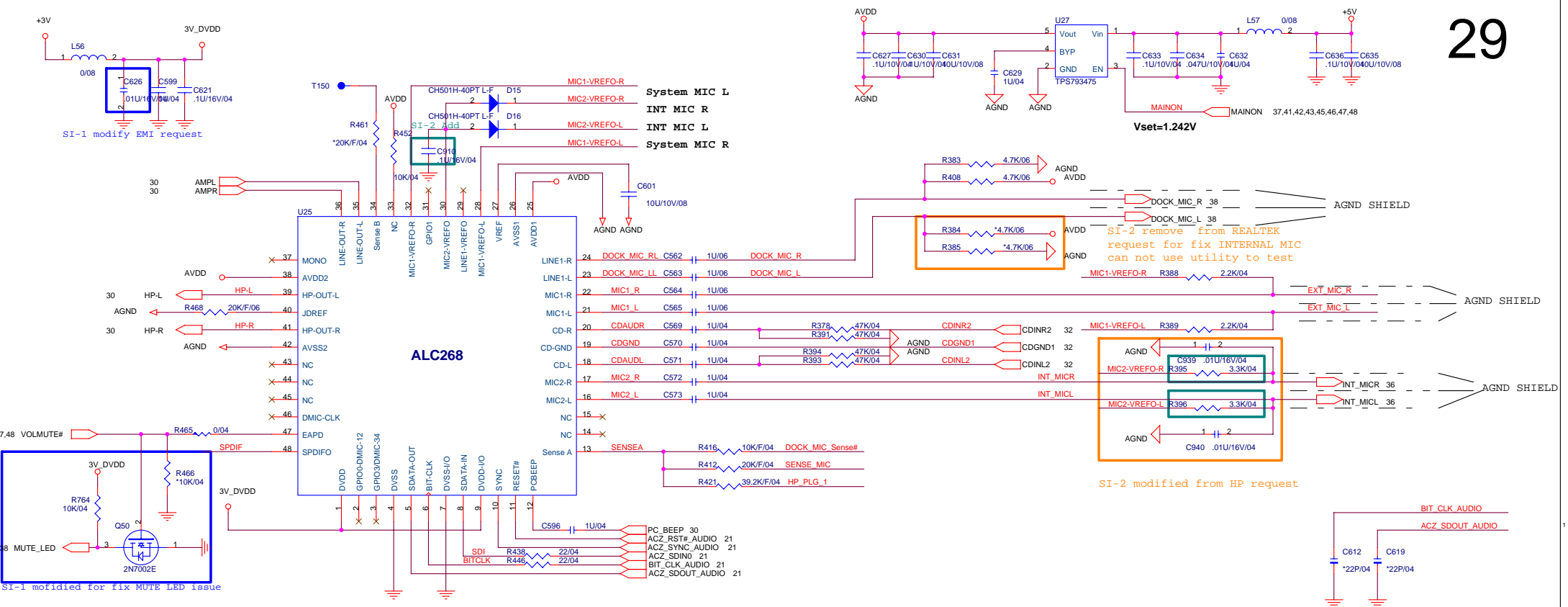
## EMI PAD



moden cable sprig

	<b>PROJECT : AT3</b>	
	Quanta Computer Inc.	
	Size Custom	Document Number CARD READER/HOLE
Date: Tuesday, January 09, 2007   Sheet 27 of 48		

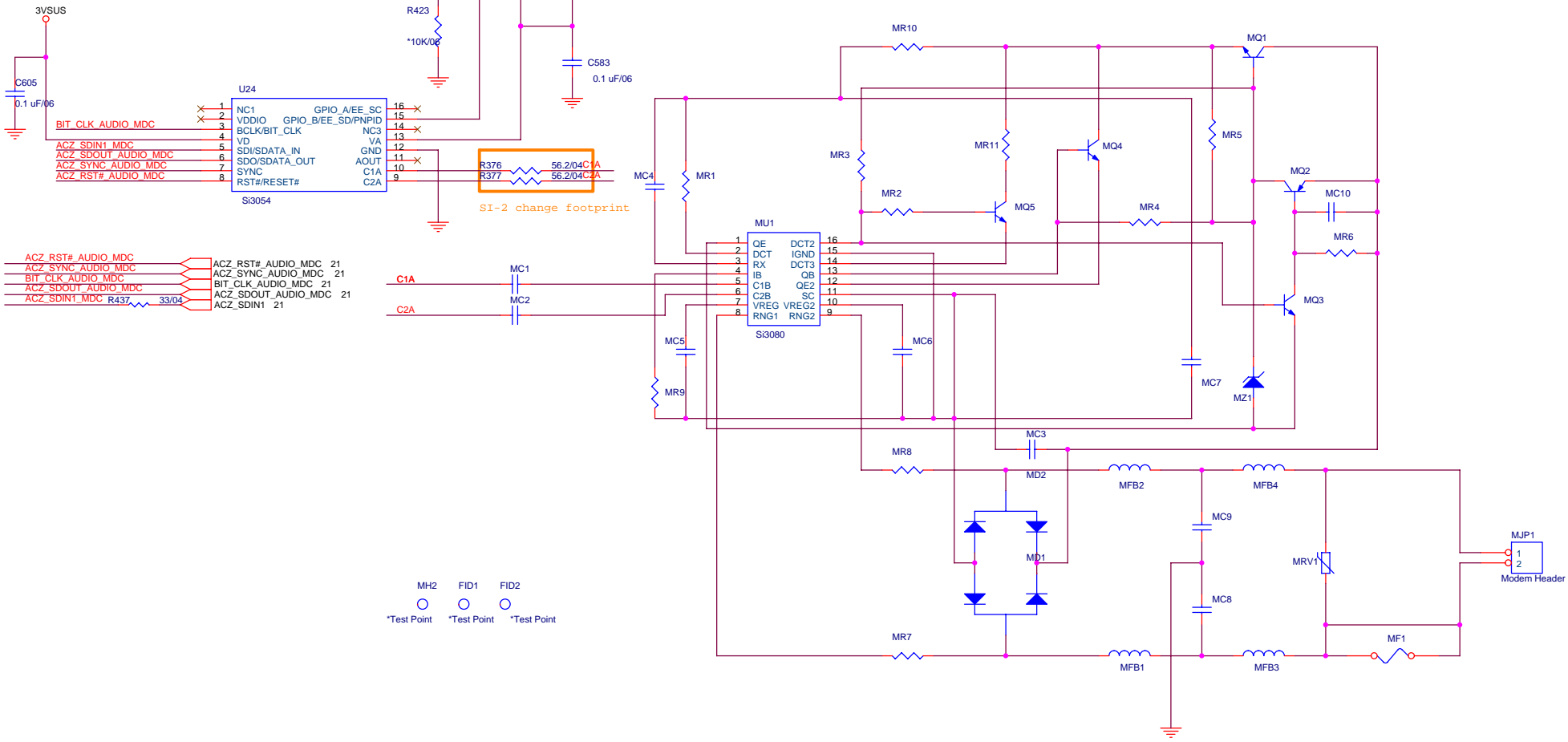







No Ground Plane In DAA Section

Homologation Area

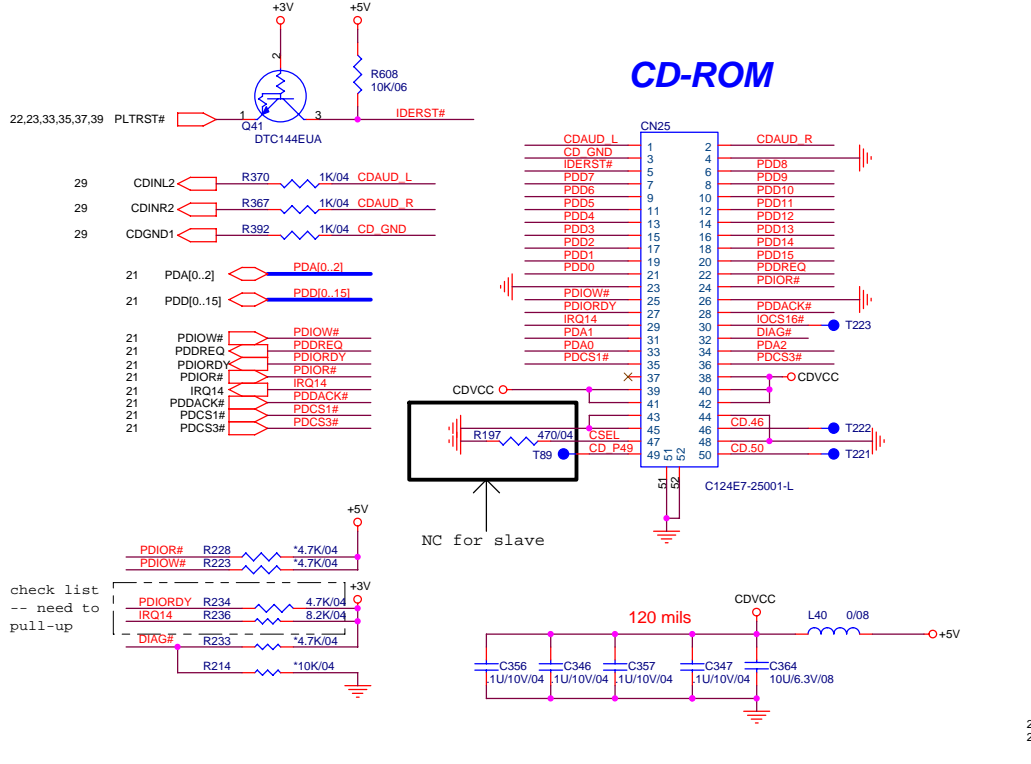


DESIGN SUBJECT TO CHANGE

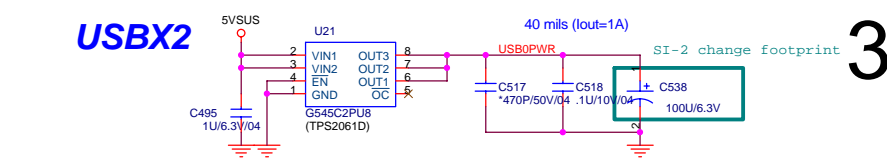
SILICON LABORATORIES CONFIDENTIAL

 NBS/RD1/HWZ	<b>PROJECT : AT3</b> <b>Quanta Computer Inc.</b>	
	Size Custom	Document Number <b>MODEM(DAA)</b>
Date: Tuesday, January 09, 2007   Sheet 31 of 48		

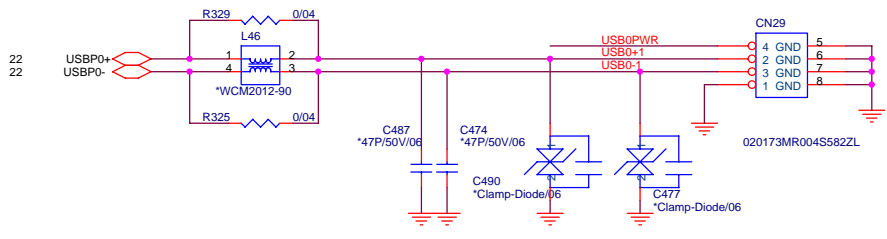
**CD-ROM**



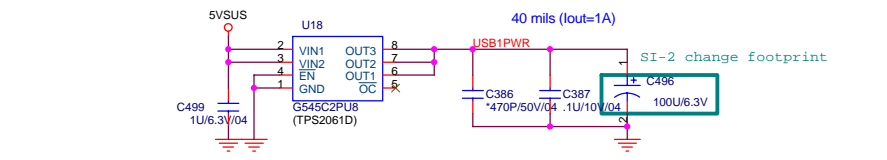
**USBX2**



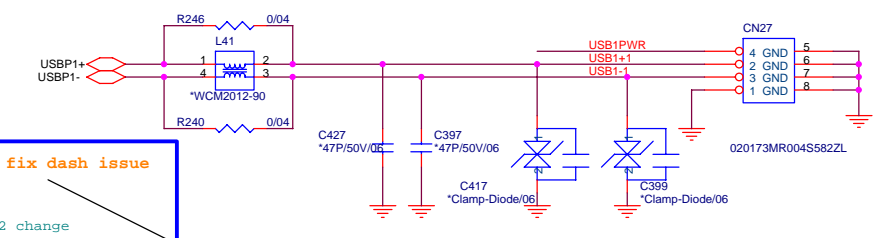
**USB 0**



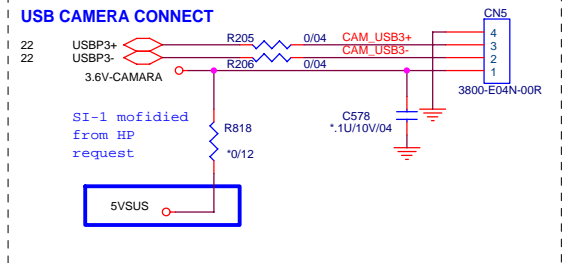
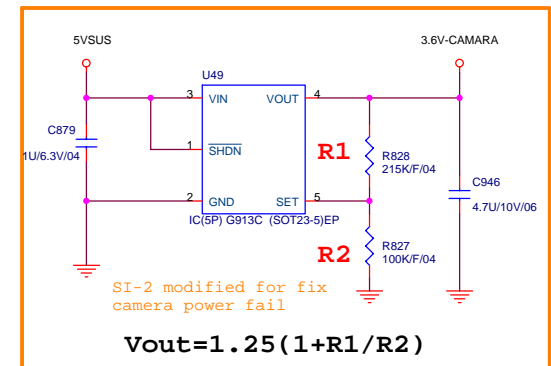
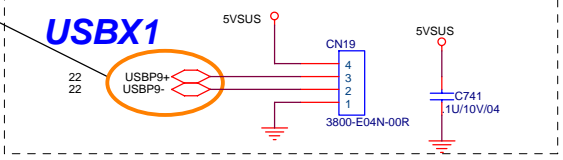
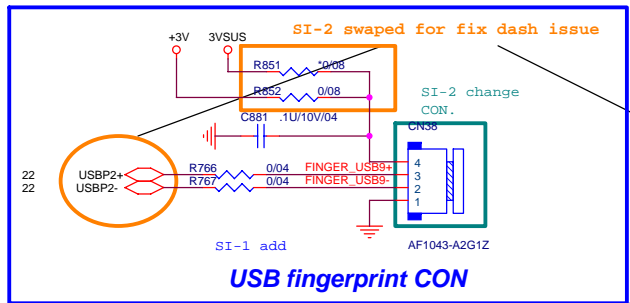
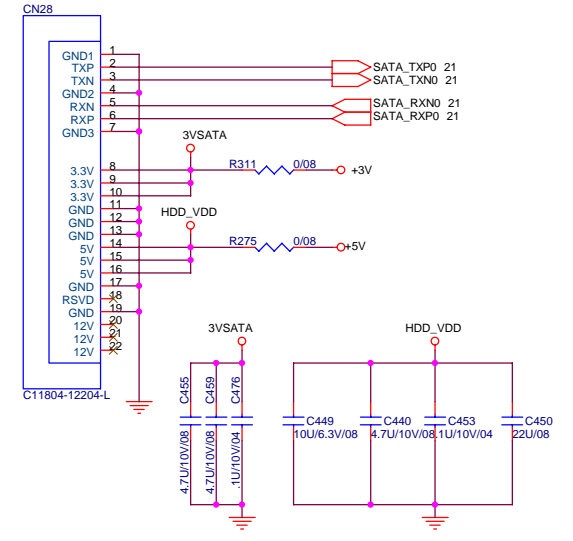
**USBX1**



**USB 1**



**SATA\_1 CONNECTOR**



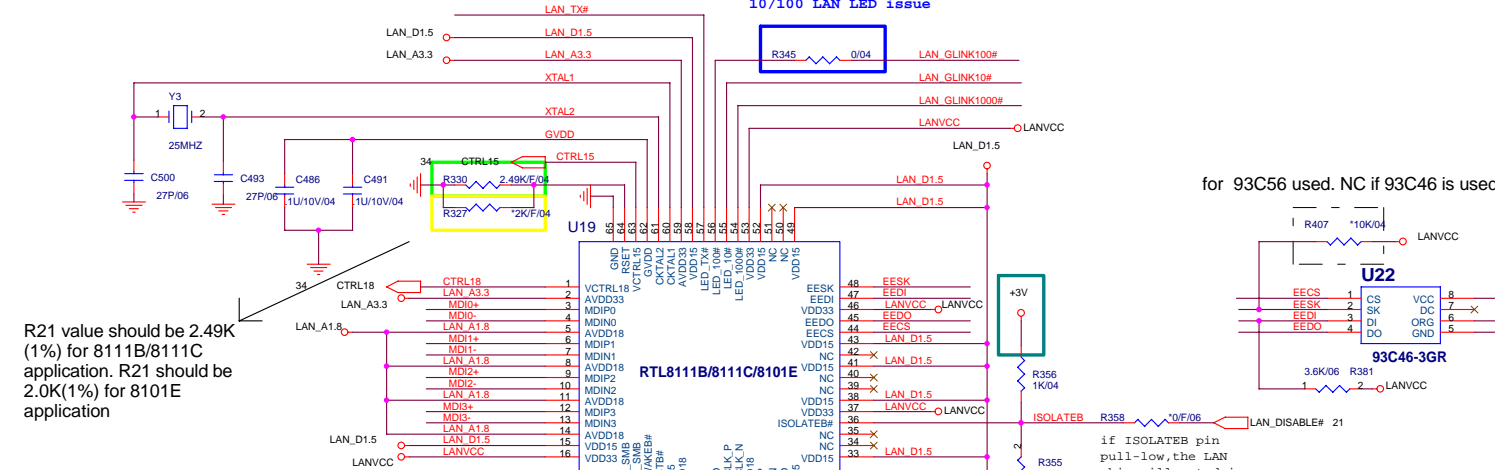


T: Stuffed for RTL8111B(10/100/1000)

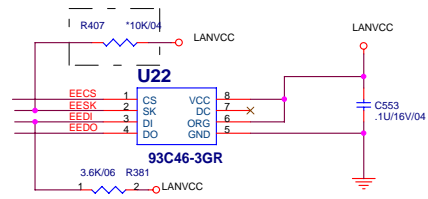
giga LAN part number AJ081110006

E: Stuffed for 8101E(10/100)

SI-1 BOM add to fix 10/100 LAN LED issue

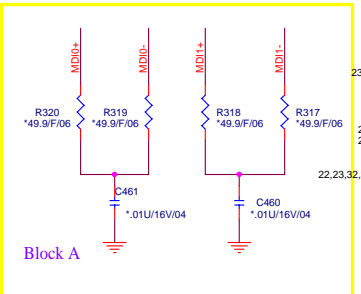


for 93C56 used. NC if 93C46 is used.

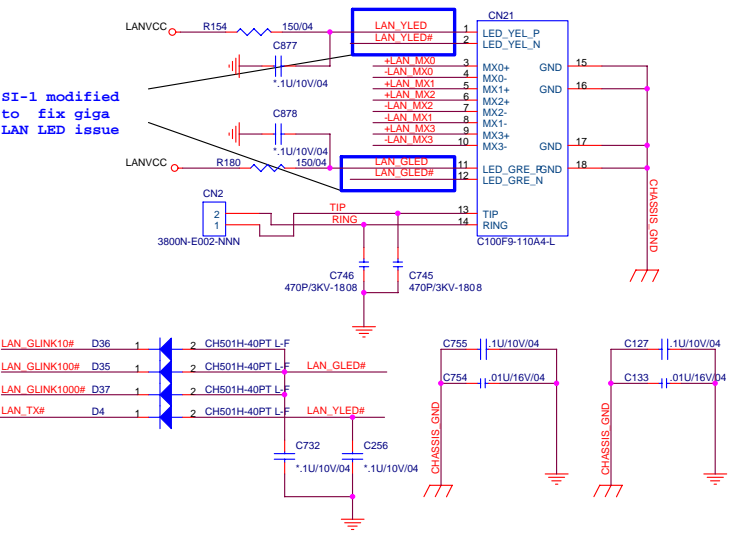


R21 value should be 2.49K (1%) for 8111B/8111C application. R21 should be 2.0K(1%) for 8101E application

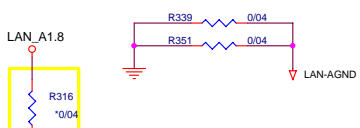
BLOCK A is only for RTL8101E application.



SI-1 modified to fix giga LAN LED issue



Remove R70 for 8111B and 8111C

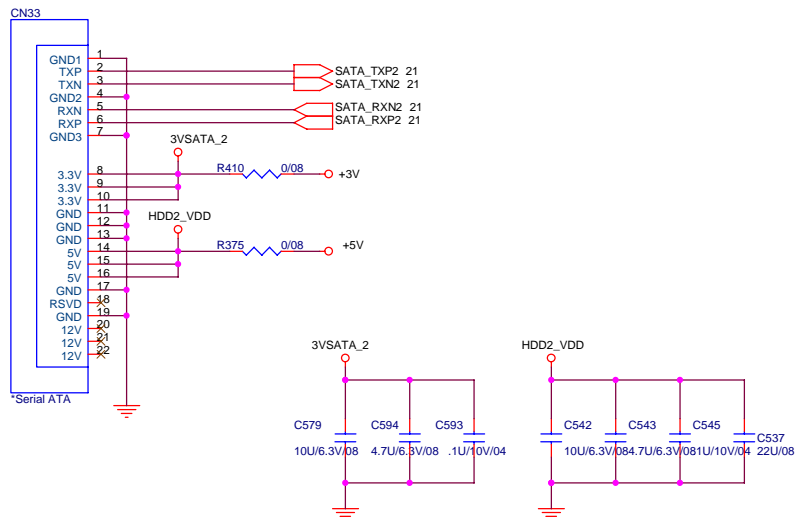


N8892403:GIGABIT N8892405:10/100

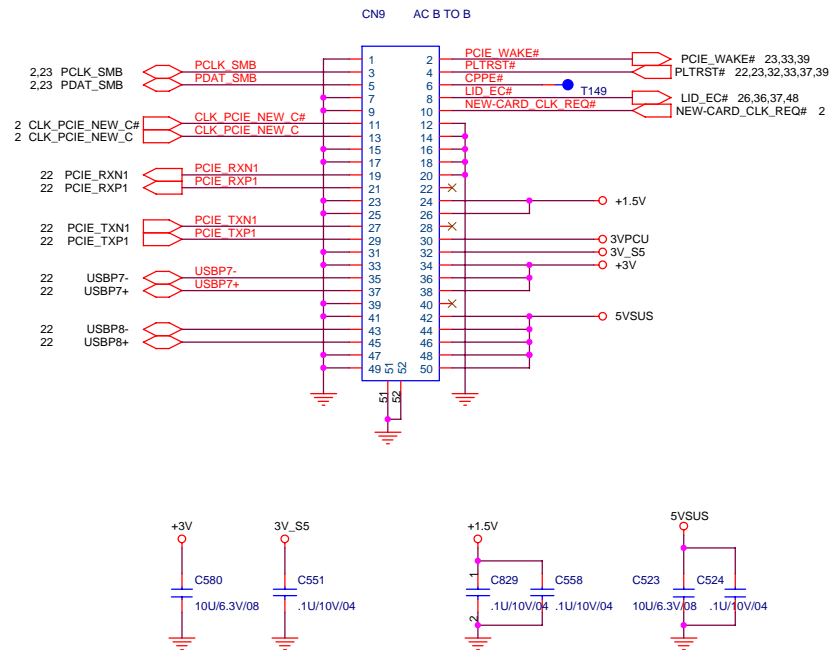


# SATA\_2 CONNECTOR

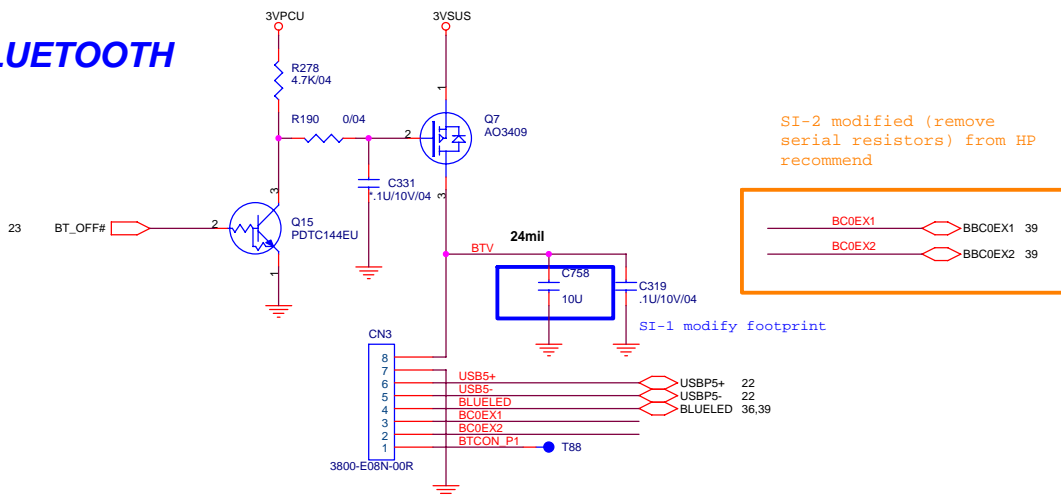
For 17" W Second HDD



# NEWCARD

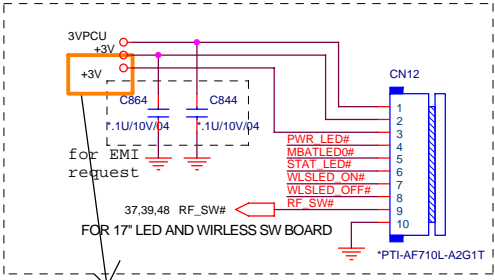


# BLUETOOTH

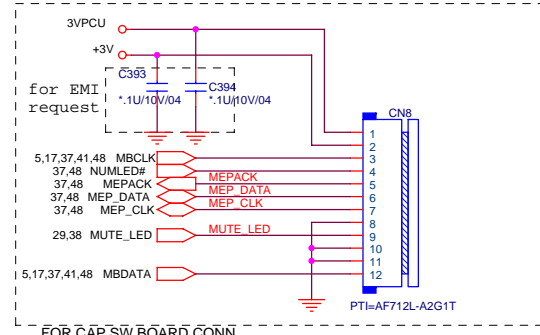


PROJECT : AT3  
Quanta Computer Inc.

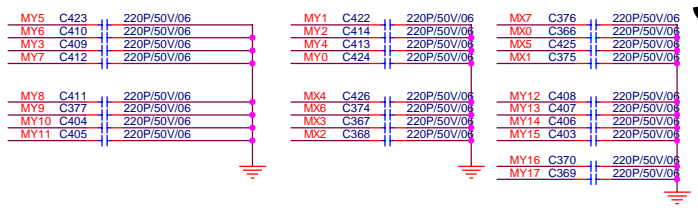
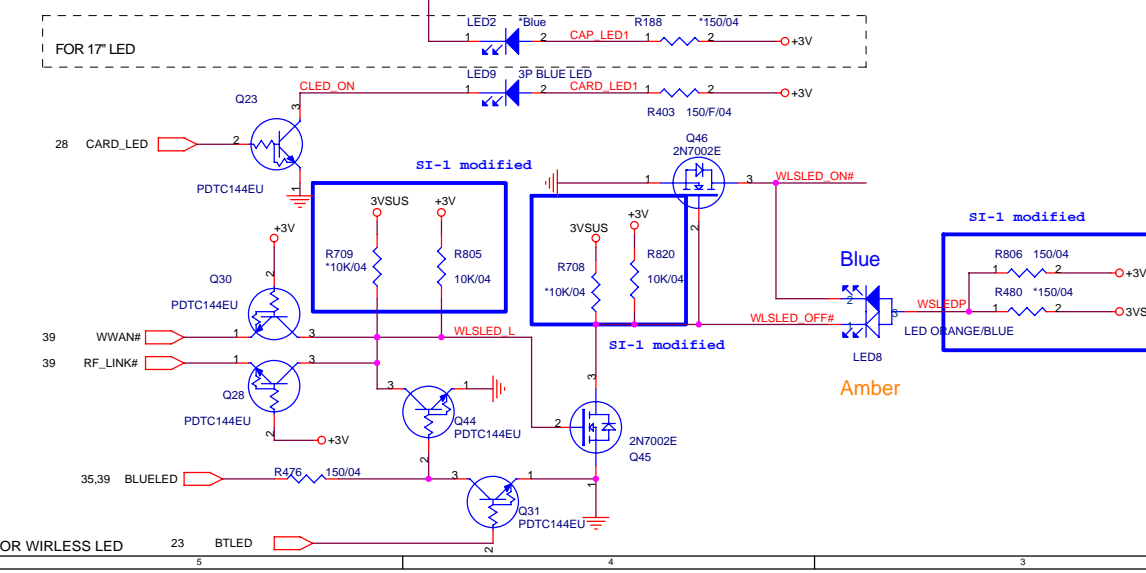
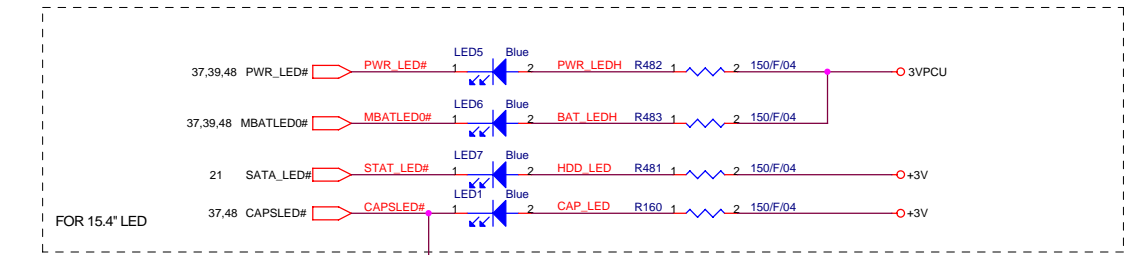
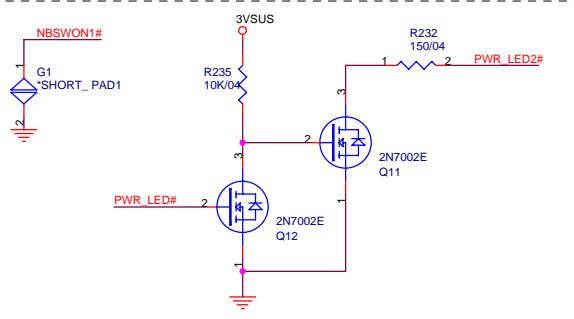
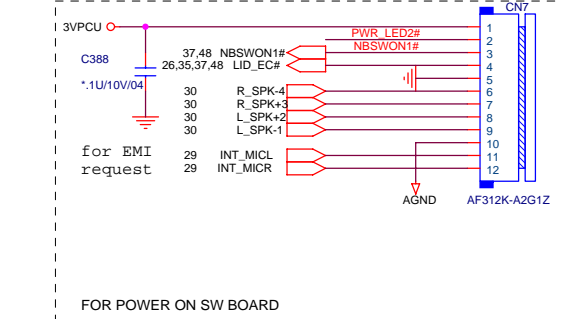
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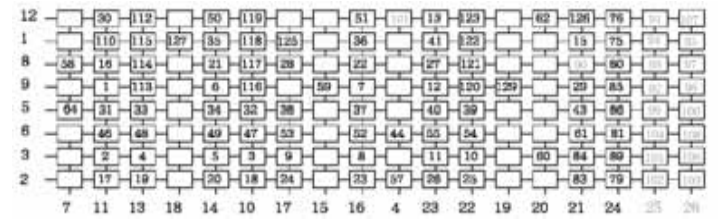
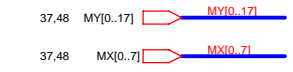
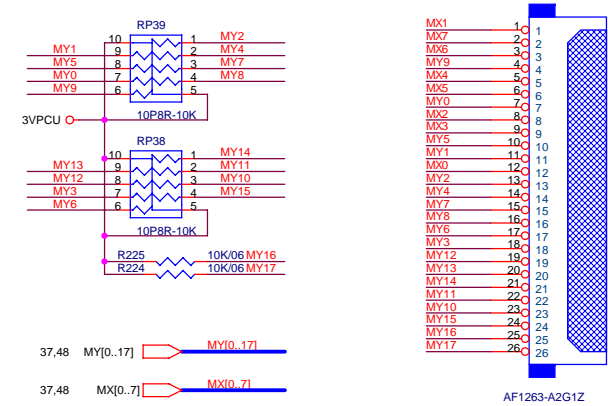
SI-2 modified for fix s3 not support wireless LED



FOR CAP SW BOARD CONN



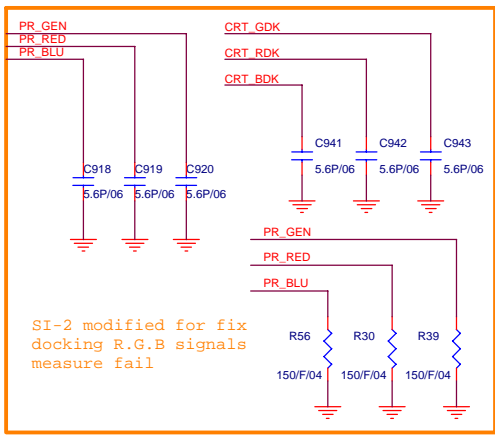
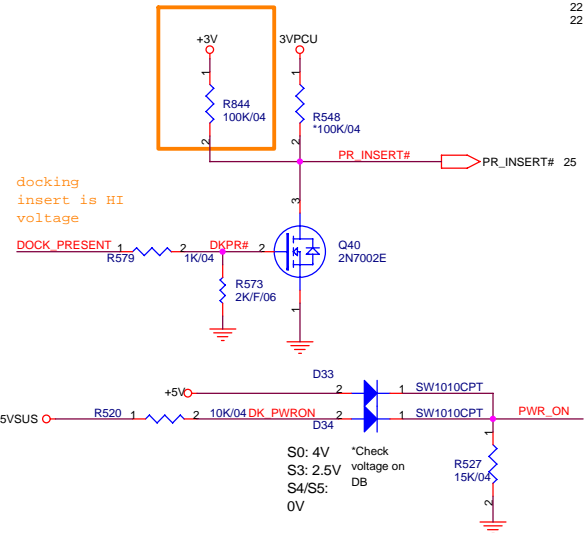
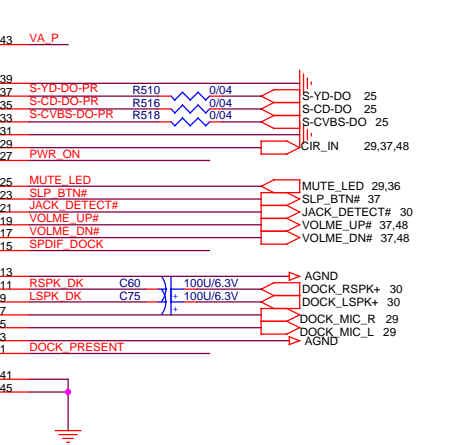
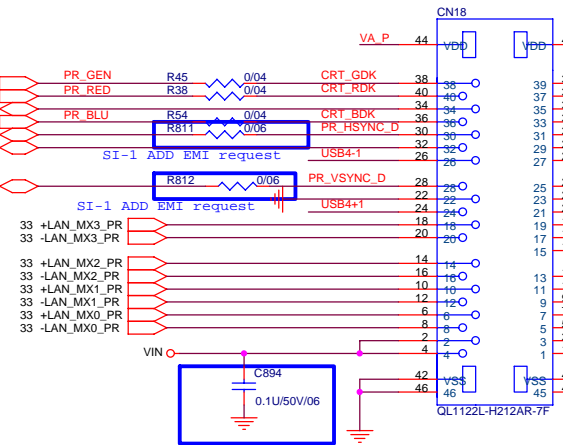
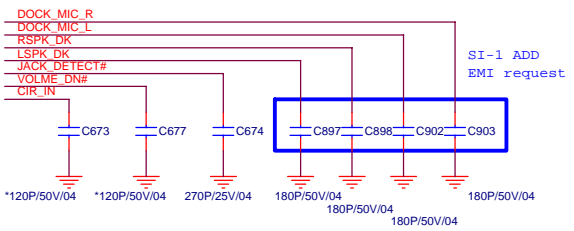
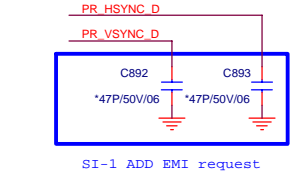
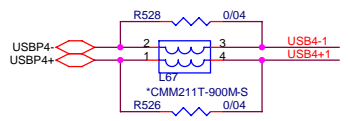
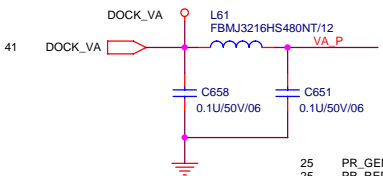
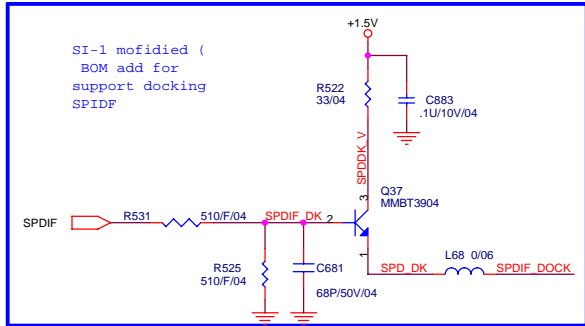
## KEYBOARD PULL-UP



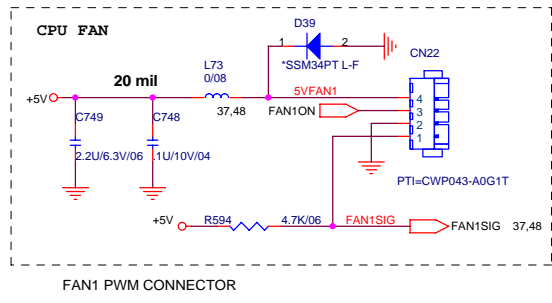
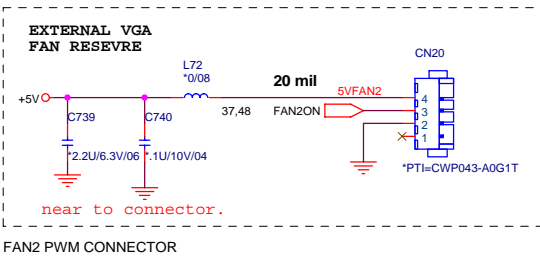


CABLE DOCK

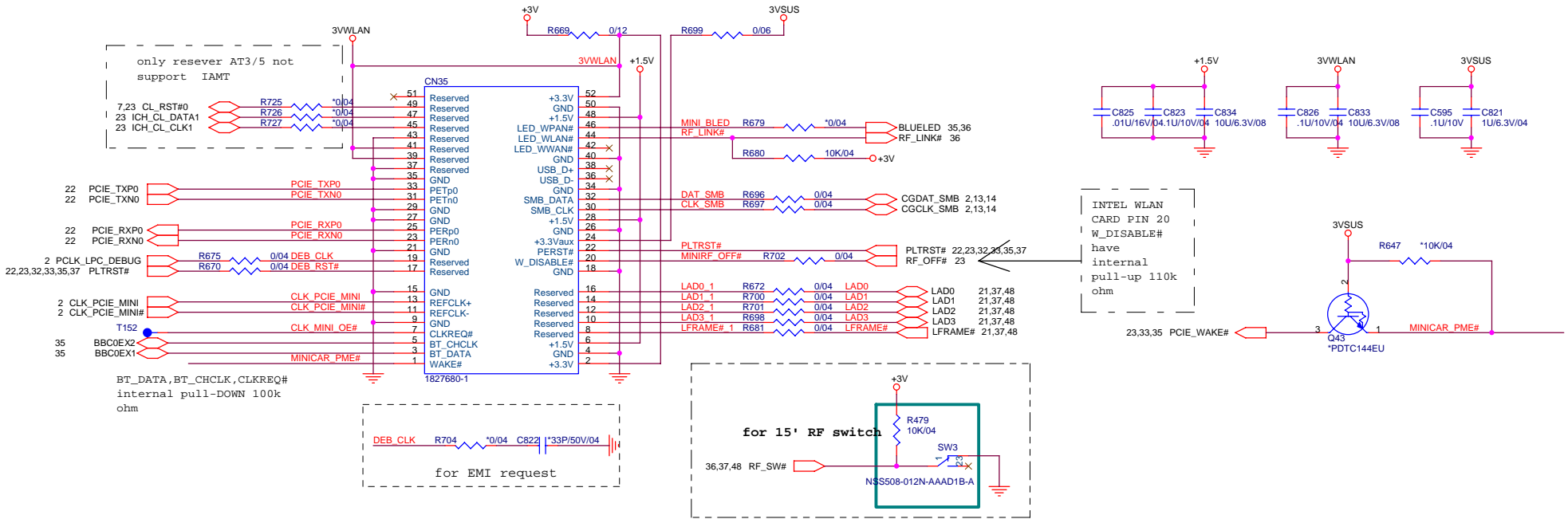
support 6A 200mils  
CX000480005



FAN

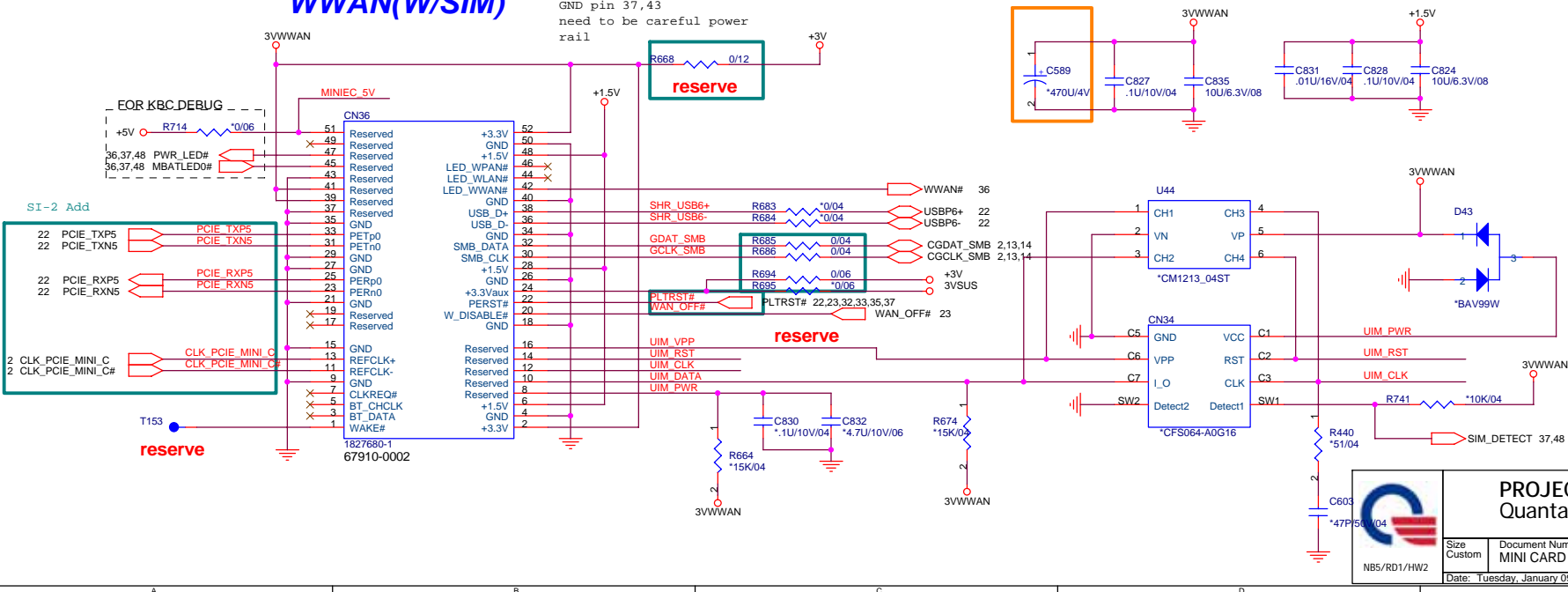


### Mini PCI-E Card 1 WLAN

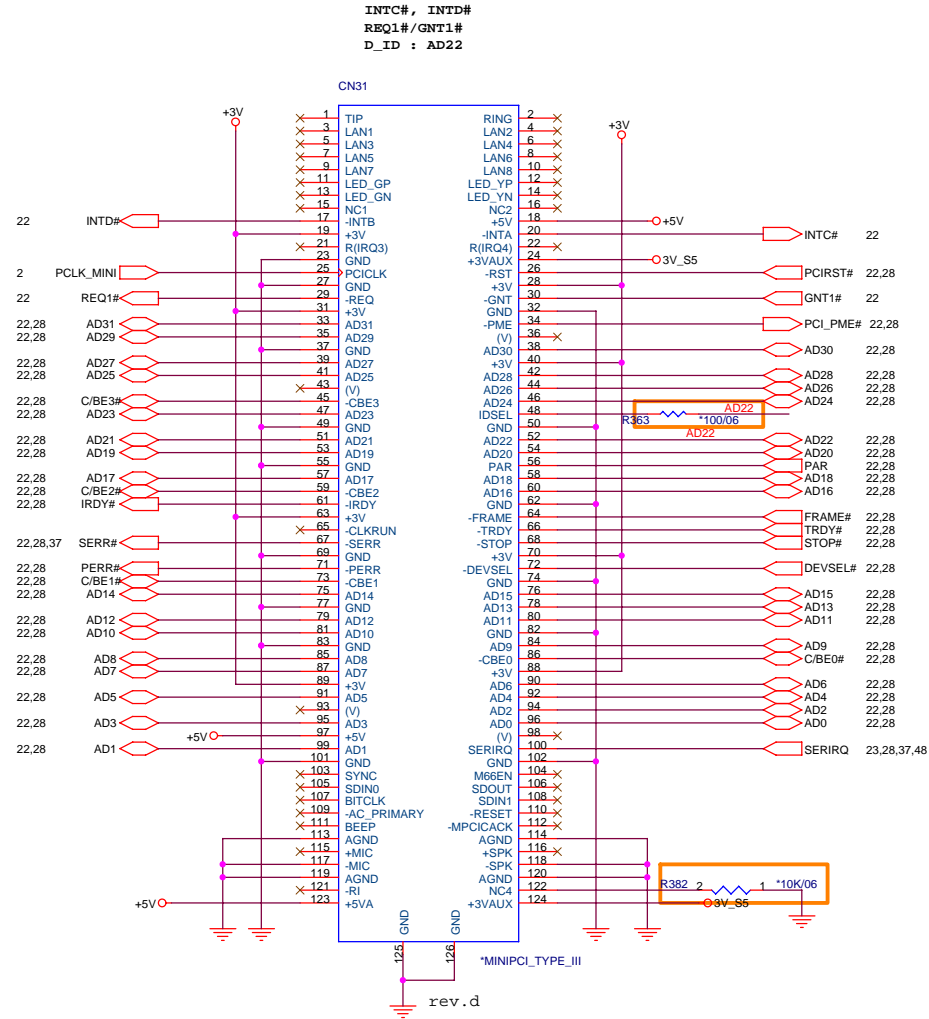



WWAN -- have 2.8A 7W power consumption  
power pin 24, 39, 41  
GND pin 37, 43  
need to be careful power rail

SI-2 modified  
(BOM remove C589)

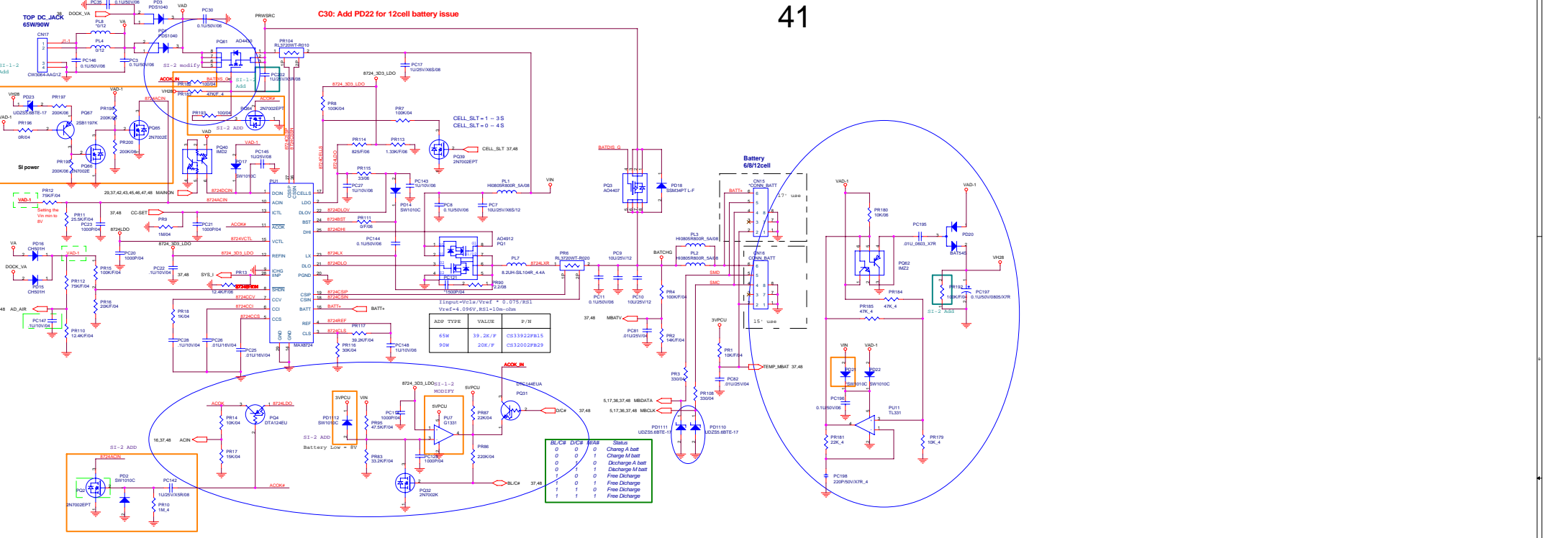


# MINI PCI TYPE III SLOT



	<b>PROJECT : AT3</b> Quanta Computer Inc.		Rev 1A
	Size Custom	Document Number MINI PCI TYPE III SLOT	Date: Tuesday, January 09, 2007





DC/DC +3V\_ALW/+5V\_ALW/+5V\_ALW2 /+12V\_ALW

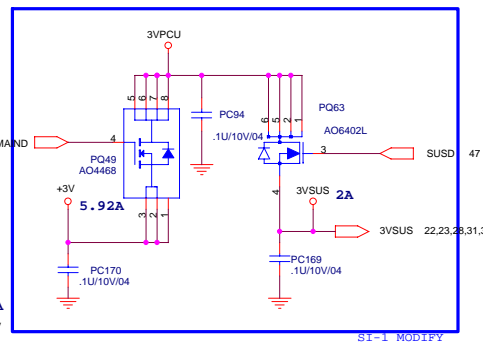
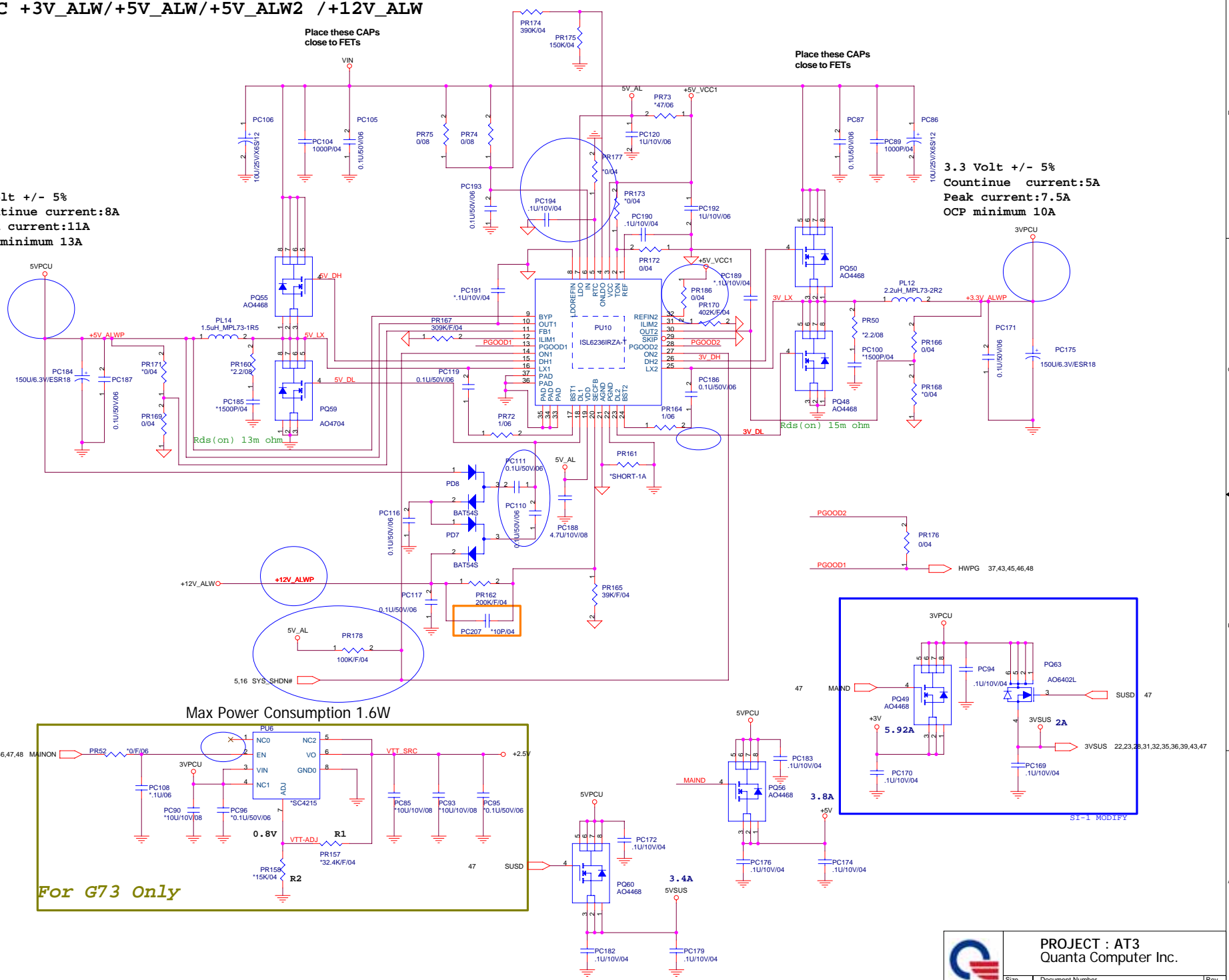
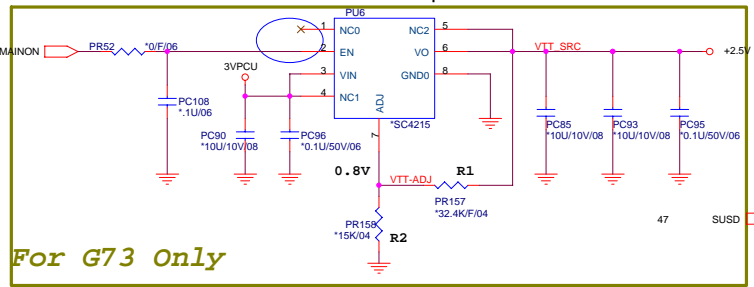
Place these CAPs close to FETs

Place these CAPs close to FETs

5 Volt +/- 5%  
 Countinue current:8A  
 Peak current:11A  
 OCP minimum 13A

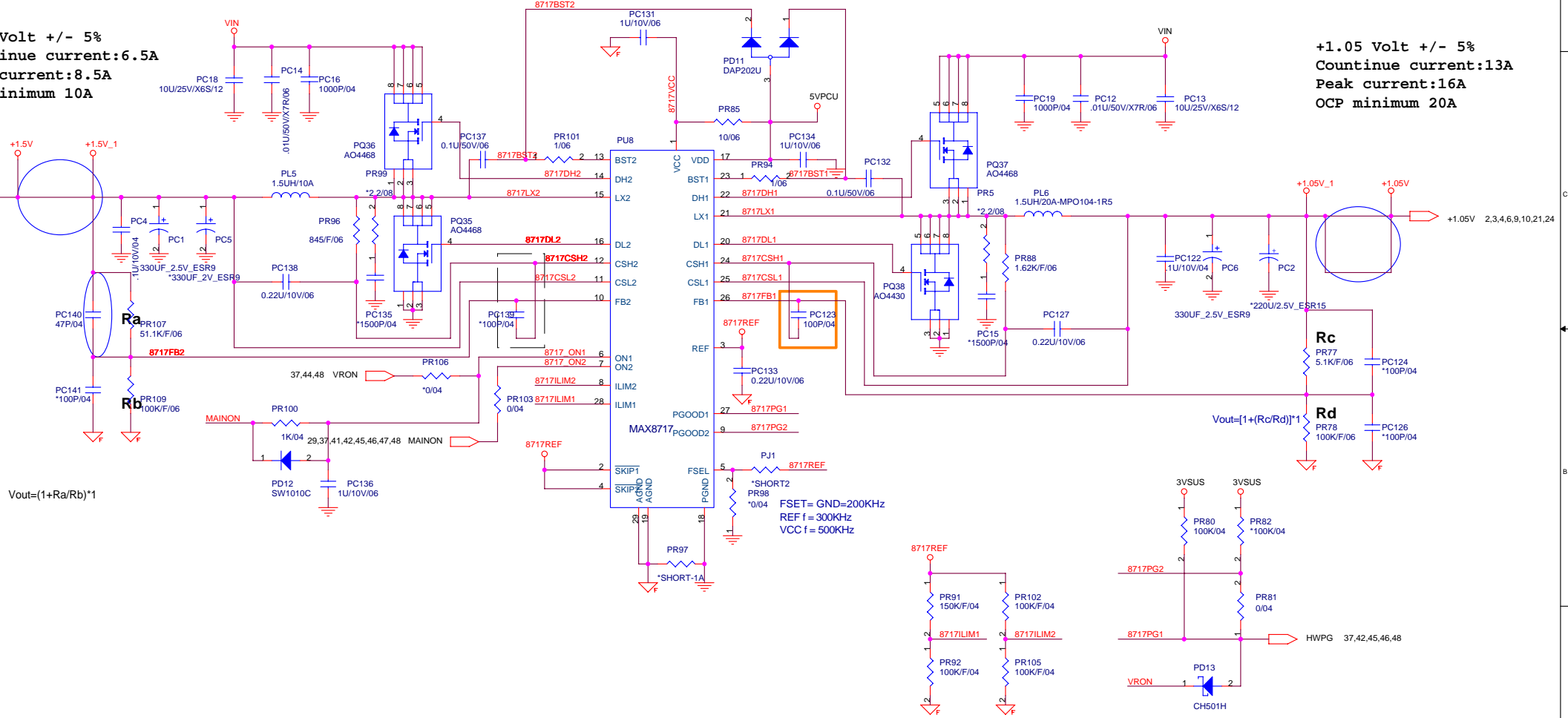
3.3 Volt +/- 5%  
 Countinue current:5A  
 Peak current:7.5A  
 OCP minimum 10A

Max Power Consumption 1.6W




+1.5 Volt +/- 5%  
Countinue current:6.5A  
Peak current:8.5A  
OCP minimum 10A

+1.05 Volt +/- 5%  
Countinue current:13A  
Peak current:16A  
OCP minimum 20A



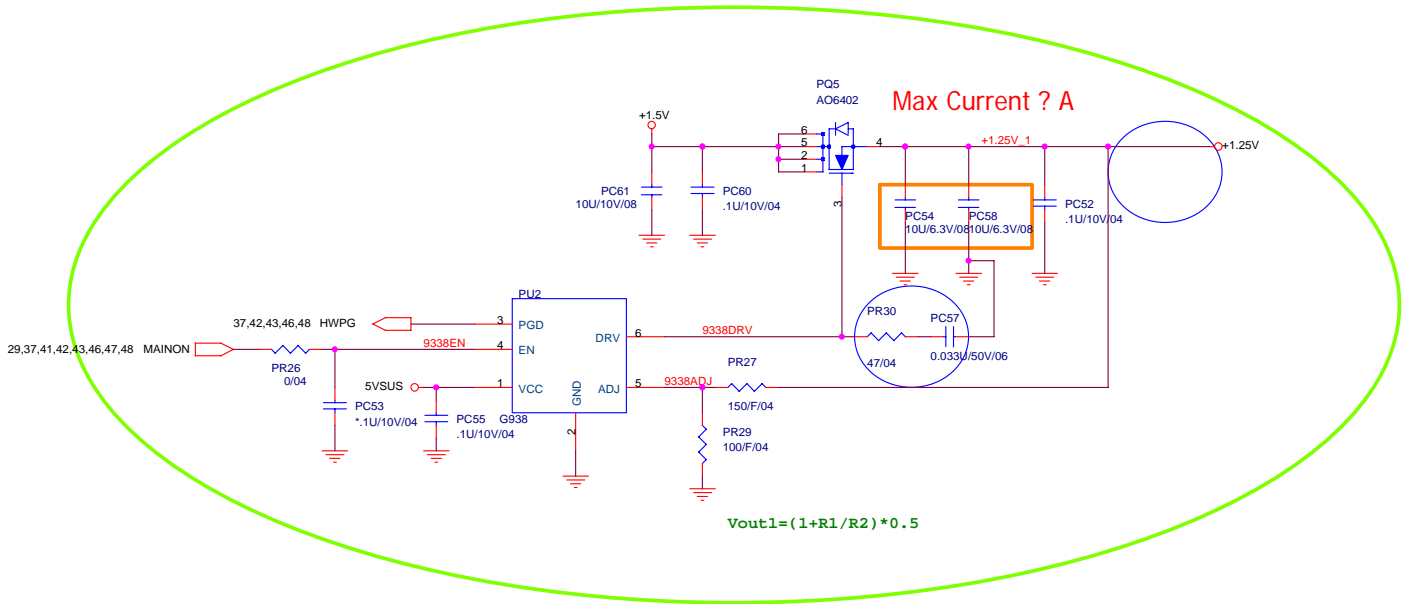
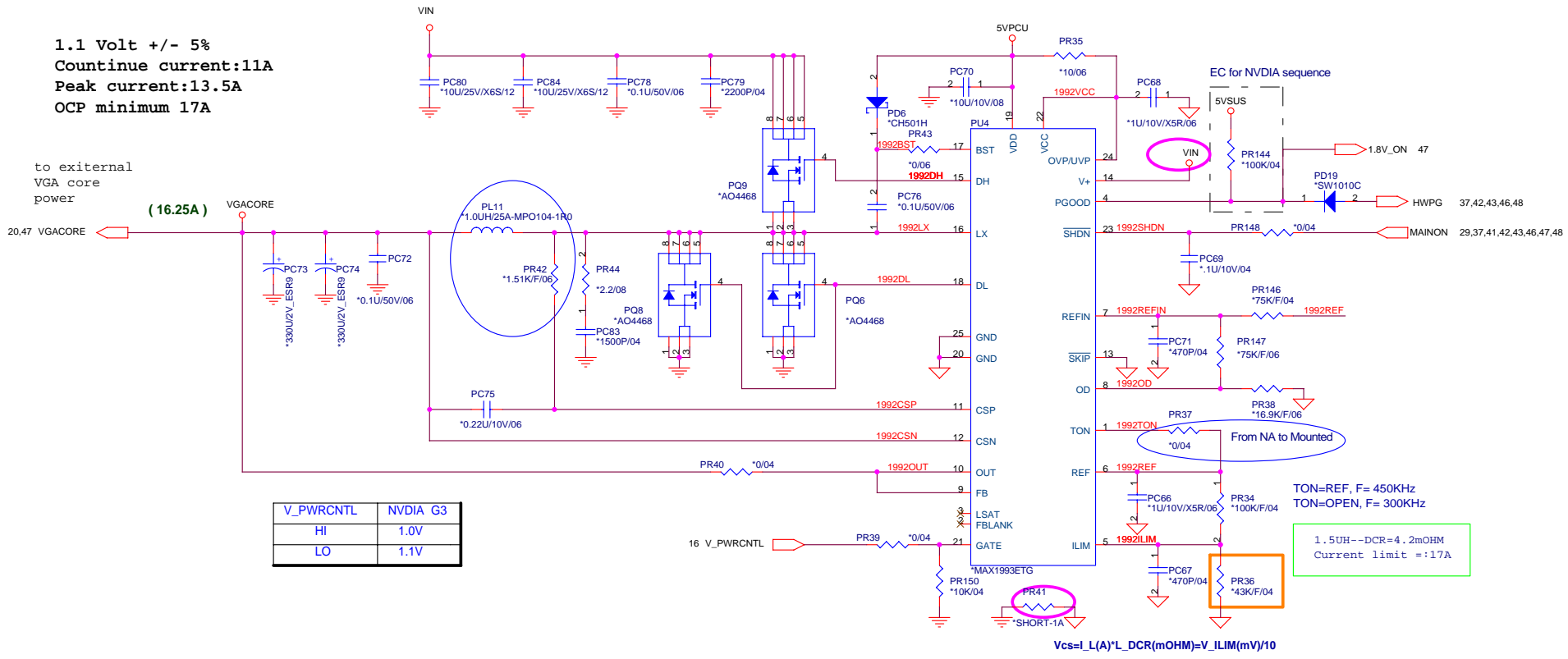
$V_{out} = (1 + R_a/R_b) * 1$

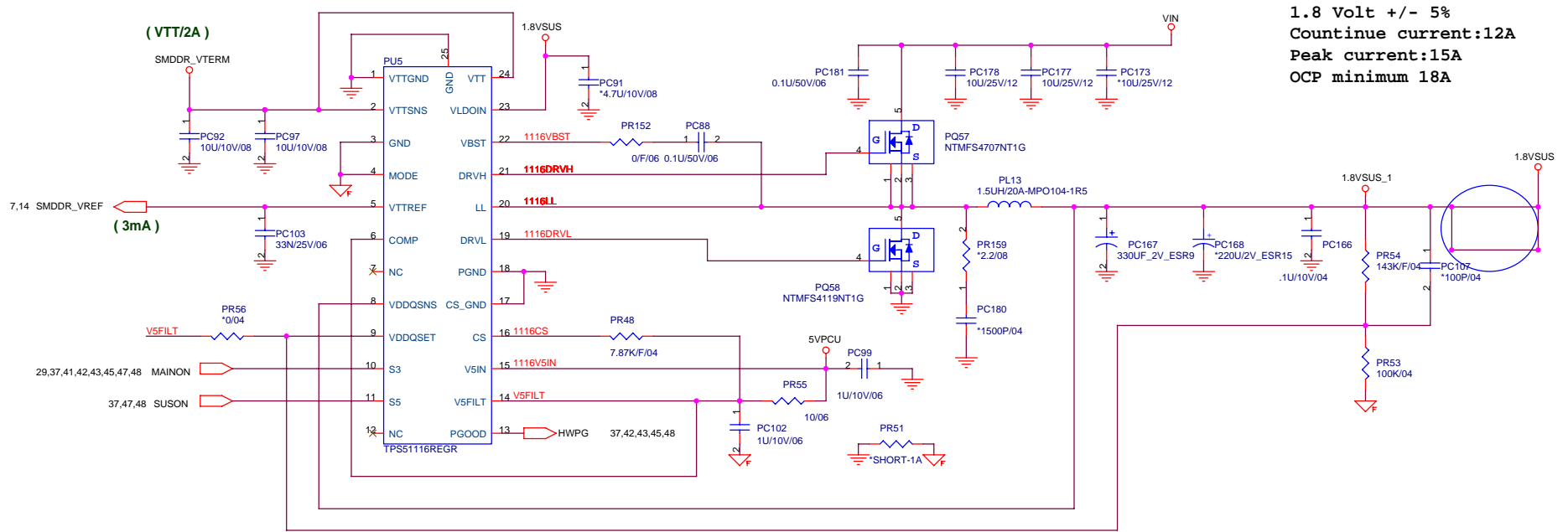
 NBS/RD1/HW2	<b>PROJECT : AT3</b> Quanta Computer Inc.		
	Size Custom	Document Number +-1.5V & VCCP+1.05V(MAX8743)	Rev 1A
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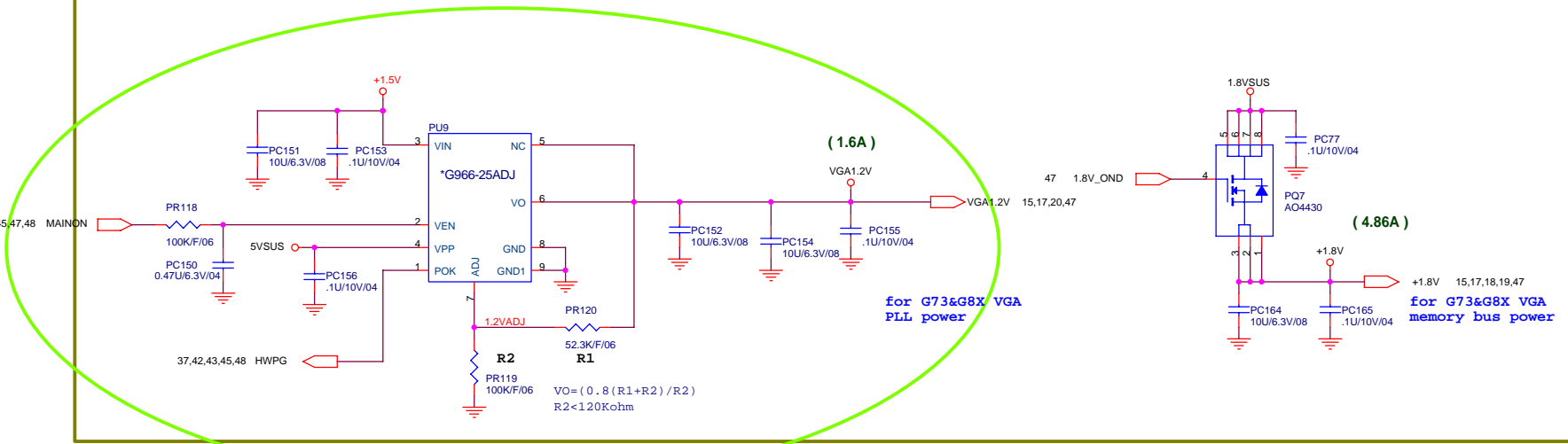
1.1 Volt +/- 5%  
 Countinue current:11A  
 Peak current:13.5A  
 OCP minimum 17A

to external  
 VGA core  
 power

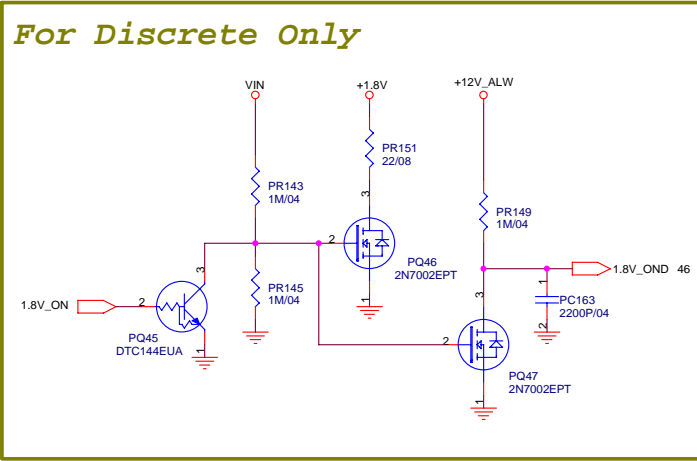
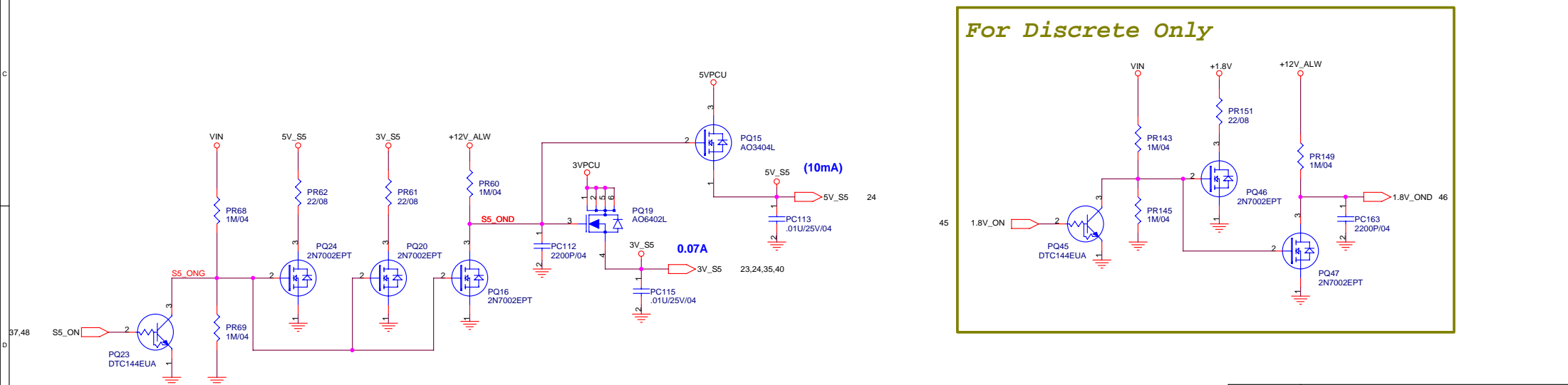
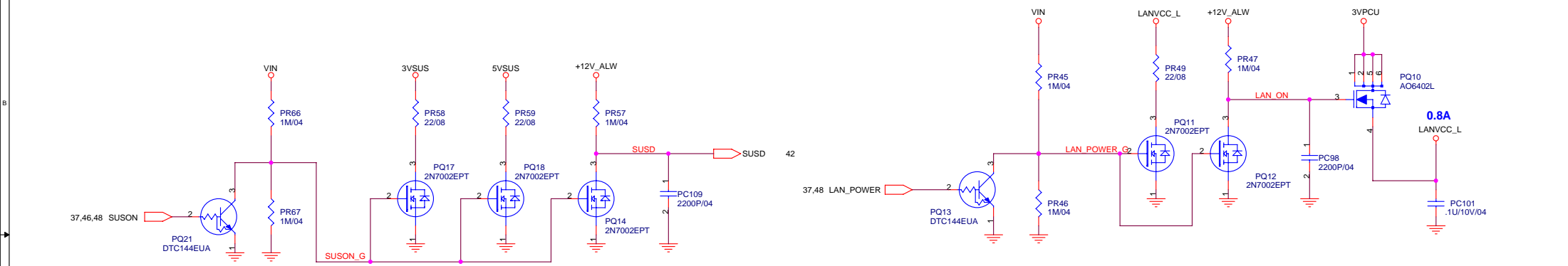
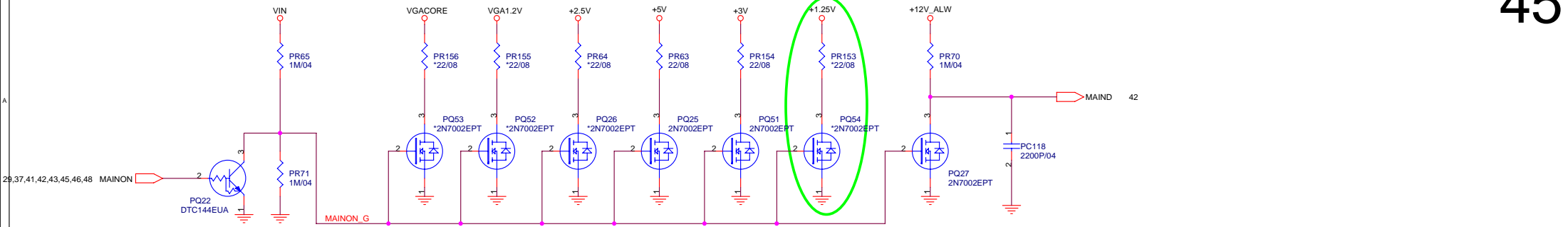


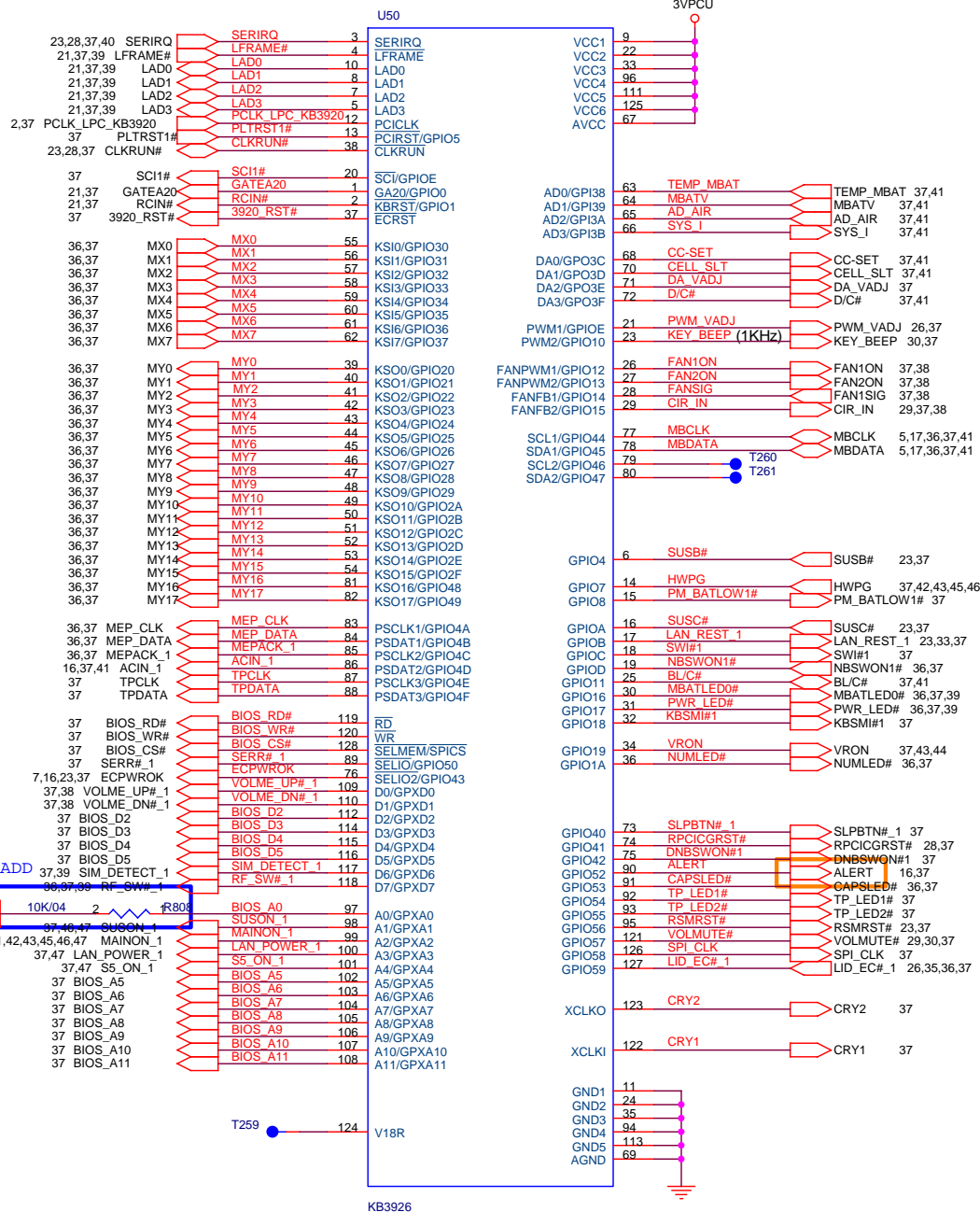


**For Discrete Only**



<b>PROJECT : AT3</b> Quanta Computer Inc.		
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SI-1 ADD



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Quanta Computer Inc.

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KB3926

T259 124

V18R



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