



# FAN6756— mWSaver™ PWM Controller

## Features

- Single-Ended Topologies, such as Flyback and Forward Converters
- mWSaver™ Technology
  - Achieves Low No-Load Power Consumption: < 30 mW at 230 V<sub>AC</sub> (EMI Filter Loss Included)
  - Eliminates X Capacitor Discharge Resistor Loss with AX-CAP® Technology
  - Linearly Decreases Switching Frequency to 23 kHz
  - Burst Mode Operation at Light-Load Condition
  - Impedance Modulation in “Deep” Burst Mode
  - Low Operating Current (450 μA) in Deep Burst Mode
  - 500 V High-Voltage JFET Startup Circuit to Eliminate Startup Resistor Loss
- Highly Integrated with Rich Features
  - Proprietary Frequency Hopping to Reduce EMI
  - High-Voltage Sampling to Detect Input Voltage
  - Peak-Current-Mode Control with Slope Compensation
  - Cycle-by-Cycle Current Limiting with Line Compensation
  - Leading Edge Blanking (LEB)
  - Built-In 7 ms Soft-Start
- Advanced Protections
  - Brown-in / Brownout Recovery
  - Internal Overload / Open-Loop Protection (OLP)
  - V<sub>DD</sub> Under-Voltage Lockout (UVLO)
  - V<sub>DD</sub> Over-Voltage Protection (V<sub>DD</sub> OVP)
  - Over-Temperature Protection (OTP)
  - Current-Sense Short-Circuit Protection (SSCP)

## Description

The FAN6756 is a next-generation Green Mode PWM controller with innovative mWSaver™ technology, which dramatically reduces standby and no-load power consumption, enabling compliance with worldwide Standby Mode efficiency guidelines.

An innovative AX-CAP® method minimizes losses in the EMI filter stage by eliminating the X-cap discharge resistors while meeting IEC61010-1 safety requirements. “Deep” Burst Mode clamps feedback voltage and modulates feedback impedance with an impedance modulator during Burst Mode operation, which forces the system to operate in a Deep Burst Mode with minimum switching losses.

Protections ensure safe operation of the power system in various abnormal conditions. A proprietary frequency-hopping function decreases EMI emission and built-in synchronized slope compensation allows more stable Peak-Current-Mode control over a wide range of input voltage and load conditions. The proprietary internal line compensation ensures constant output power limit over the entire universal line voltage range.

Requiring a minimum number of external components, FAN6756 provides a basic platform that is well suited for cost-effective flyback converter designs that require extremely low standby power consumption.

## Applications

Flyback power supplies that demand extremely low standby power consumption, such as:

- Adapters for Notebooks, Printers, Game Consoles, etc.
- Open-Frame SMPS for LCD TV, LCD Monitors, Printer Power, etc.

## Related Resources

- [Evaluation Board: FEBFAN6756MR\\_T03U065A](#)

## Ordering Information

| Part Number | Protections <sup>(1)</sup> |     |     |      | Operating Temperature Range | Package                            | Packing Method |
|-------------|----------------------------|-----|-----|------|-----------------------------|------------------------------------|----------------|
|             | OLP                        | OVP | OTP | SSCP |                             |                                    |                |
| FAN6756MRMY | A/R                        | L   | L   | A/R  | -40 to +105°C               | 8-Pin, Small Outline Package (SOP) | Tape & Reel    |
| FAN6756MLMY | L                          | L   | L   | A/R  |                             |                                    |                |

### Note:

1. A/R = Auto Recovery Mode protection, L = Latch Mode protection.

### Application Diagram

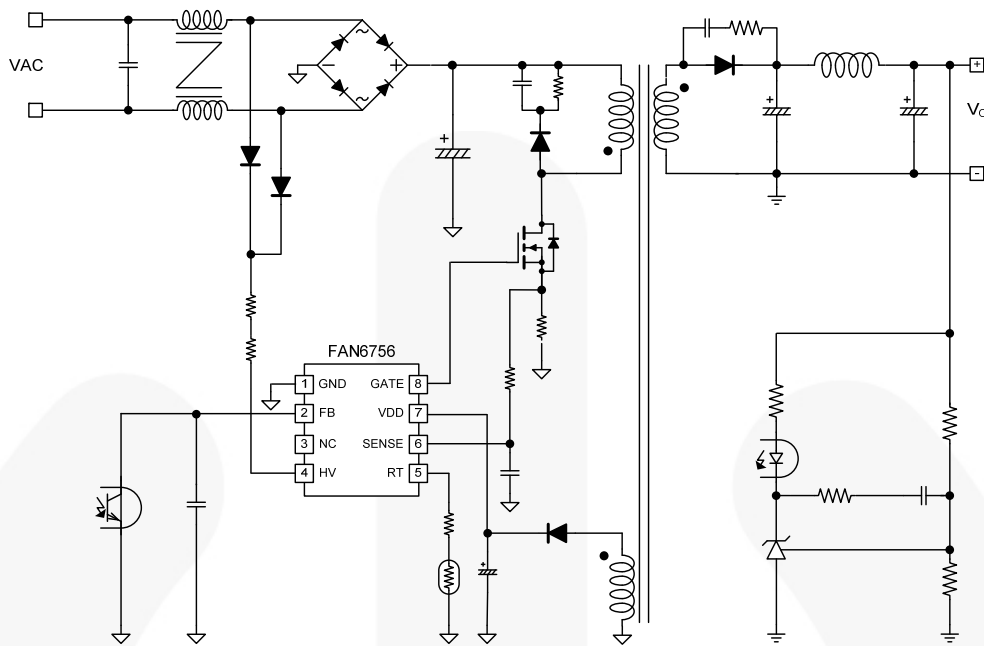


Figure 1. Typical Application

### Internal Block Diagram

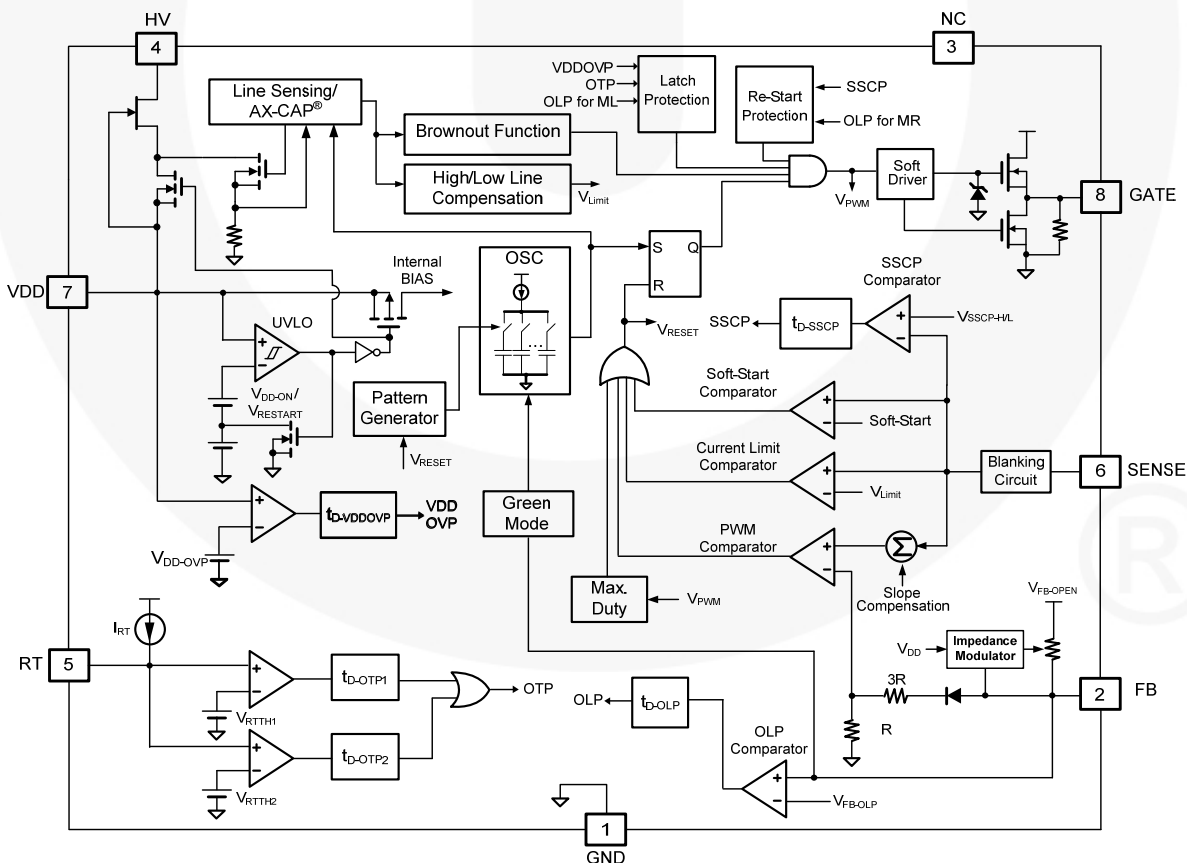


Figure 2. Functional Block Diagram

## Marking Information

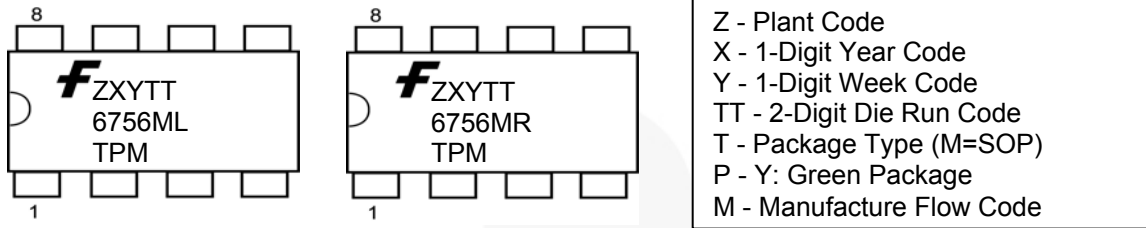


Figure 3. Top Mark

## Pin Configuration

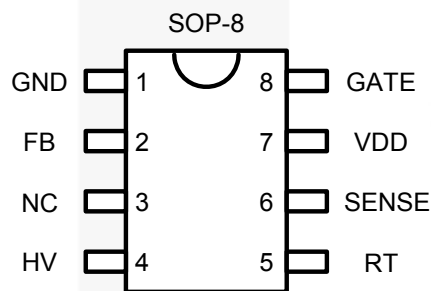


Figure 4. Pin Configuration (Top View)

## Pin Definitions

| Pin # | Name  | Description  |
|-------|-------|--|
| 1     | GND   | Ground. Placing a 0.1 $\mu$ F decoupling capacitor between VDD and GND is recommended.   |
| 2     | FB    | Feedback. The output voltage feedback information from the external compensation circuit is fed into this pin. The PWM duty cycle is determined by comparing the FB signal with the current-sense signal from the SENSE pin.   |
| 3     | NC    | No Connection  |
| 4     | HV    | High-Voltage Startup. The HV pin is typically connected to the AC line input through two external diodes and one resistor ( $R_{HV}$ ). This pin is used, not only to charge the $V_{DD}$ capacitor during startup, but also to sense the line voltage. The line voltage information is used for brownout protection and power-limit line compensation. This pin also is used to intelligently discharge the EMI filter capacitor when removal of the AC line voltage is detected. |
| 5     | RT    | Over-Temperature Protection. An external NTC thermistor is connected from this pin to GND. Once the voltage of the RT pin drops below the threshold voltage, the controller latches off the PWM. The RT pin also provides external latch protection. If the RT pin is not connected to the NTC resistor for over-temperature protection, it is recommended to place a 100 k $\Omega$ resistor to ground to prevent noise interference.   |
| 6     | SENSE | Current Sense. The sensed voltage is used for Peak-Current-Mode control, short-circuit protection, and cycle-by-cycle current limiting.  |
| 7     | VDD   | Power Supply of IC. Typically a hold-up capacitor connects from this pin to ground. A rectifier diode, in series with the transformer auxiliary winding, connects to this pin to supply bias during normal operation.  |
| 8     | GATE  | Gate Drive Output. The totem-pole output driver for the power MOSFET; internally limited to $V_{GATE-CLAMP}$ .   |

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol             | Parameter   |                                       | Min. | Max. | Unit |
|--------------------|---|---------------------------------------|------|------|------|
| V <sub>VDD</sub>   | DC Supply Voltage <sup>(2,3)</sup>                  |                                       |      | 30   | V    |
| V <sub>FB</sub>    | FB Pin Input Voltage                                |                                       | -0.3 | 7.0  | V    |
| V <sub>SENSE</sub> | SENSE Pin Input Voltage                             |                                       | -0.3 | 7.0  | V    |
| V <sub>RT</sub>    | RT Pin Input Voltage                                |                                       | -0.3 | 7.0  | V    |
| V <sub>HV</sub>    | HV Pin Input Voltage                                |                                       |      | 500  | V    |
| P <sub>D</sub>     | Power Dissipation (T <sub>A</sub> < 50°C)           |                                       |      | 400  | mW   |
| Θ <sub>JA</sub>    | Thermal Resistance (Junction-to-Air)                |                                       |      | 150  | °C/W |
| T <sub>J</sub>     | Operating Junction Temperature                      |                                       | -40  | +125 | °C   |
| T <sub>STG</sub>   | Storage Temperature Range                           |                                       | -55  | +150 | °C   |
| T <sub>L</sub>     | Lead Temperature (Wave Soldering or IR, 10 Seconds) |                                       |      | +260 | °C   |
| ESD                | Human Body Model,<br>JEDEC:JESD22-A114              | All Pins Except HV Pin <sup>(4)</sup> |      | 6000 | V    |
|                    | Charged Device Model,<br>JEDEC:JESD22-C101          | All Pins Except HV Pin <sup>(4)</sup> |      | 2000 |      |

### Notes:

- All voltage values, except differential voltages, are given with respect to the network ground terminal.
- Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.
- ESD level on HV pin is CDM=1250 V and HBM=500 V.

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. We does not recommend exceeding them or designing to Absolute Maximum Ratings.

| Symbol          | Parameter            | Min. | Typ. | Max. | Unit |
|-----------------|----------------------|------|------|------|------|
| R <sub>HV</sub> | Resistance on HV Pin | 150  | 200  | 250  | kΩ   |

## Electrical Characteristics

$V_{DD}=15\text{ V}$  and  $T_J=T_A=25^\circ\text{C}$  unless otherwise noted.

| Symbol                        | Parameter   | Condition  | Min.             | Typ.           | Max.             | Unit          |               |
|-------------------------------|---|--|------------------|----------------|------------------|---------------|---------------|
| <b>V<sub>DD</sub> Section</b> |   |  |                  |                |                  |               |               |
| $V_{DD-ON}$                   | Threshold Voltage to Startup  | $V_{DD}$ Rising  | 16               | 17             | 18               | V             |               |
| $V_{UVLO}$                    | Threshold Voltage to Stop Switching in Normal Mode                            | $V_{DD}$ Falling   | 5.5              | 6.5            | 7.5              | V             |               |
| $V_{RESTART}$                 | Threshold Voltage to Enable HV Startup to Charge $V_{DD}$ in Normal Mode      | $V_{DD}$ Falling   |                  | 4.7            |                  | V             |               |
| $V_{DD-OFF}$                  | Threshold Voltage to Stop Operating in Protection Mode                        | $V_{DD}$ Falling   | 10               | 11             | 12               | V             |               |
| $V_{DD-OLP}$                  | Threshold Voltage to Enable HV Startup to Charge $V_{DD}$ in Protection Mode  | $V_{DD}$ Falling   | 6                | 7              | 8                | V             |               |
| $V_{DD-LH}$                   | Threshold Voltage to Release Latch Mode                                       | $V_{DD}$ Falling   | 3.5              | 4.0            | 4.5              | V             |               |
| $V_{DD-AC}$                   | Threshold Voltage of VDD pin for Enabling Brown-in                            |  | $V_{UVLO} + 2.5$ | $V_{UVLO} + 3$ | $V_{UVLO} + 3.5$ | V             |               |
| $I_{DD-ST}$                   | Startup Current   | $V_{DD}=V_{DD-ON} - 0.16\text{ V}$   |                  |                | 30               | $\mu\text{A}$ |               |
| $I_{DD-OP1}$                  | Supply Current in PWM Operation   | $V_{DD}=15\text{ V}$ , $V_{FB} = 3\text{ V}$ , Gate Open                   |                  |                | 1.8              | mA            |               |
| $I_{DD-OP2}$                  | Supply Current when PWM Stops   | $V_{DD}=15\text{ V}$ , $V_{FB} < 1.4\text{ V}$ , Deep Burst Mode, Gate Off |                  | 450            |                  | $\mu\text{A}$ |               |
| $I_{DD-OLP}$                  | Internal Sink Current, $V_{DD-OLP} < V_{DD} < V_{DD-OFF}$ , Protection Mode   | $V_{DD}=$  | FAN6756MRMY      | 90             | 140              | 190           | $\mu\text{A}$ |
|                               |   | $V_{DD-OLP} + 0.1\text{ V}$  | FAN6756MLMY      | 160            | 210              | 260           | $\mu\text{A}$ |
| $I_{LH}$                      | Internal Sink Current, $V_{DD} < V_{DD-OLP}$ , Latch-Protection Mode          | $V_{DD} = 5\text{ V}$  | 30               |                |                  | $\mu\text{A}$ |               |
| $V_{DD-OVP}$                  | Threshold Voltage for $V_{DD}$ Over-Voltage Protection                        |  | 23.5             | 24.5           | 25.5             | V             |               |
| $t_{D-VDDOVP}$                | $V_{DD}$ Over-Voltage Protection Debounce Time                                |  | 110              | 205            | 300              | $\mu\text{s}$ |               |
| $V_{DD-ZFBR}$                 | $V_{DD}$ Threshold Voltage for FB-Pin Impedance Modulation in Deep Burst Mode |  |                  | 7              |                  | V             |               |

Continued on the following page...

**Electrical Characteristics** (Continued)V<sub>DD</sub>=15 V and T<sub>J</sub>=T<sub>A</sub>=25°C unless otherwise noted.

| Symbol                    | Parameter  | Condition   | Min.                                    | Typ.                                    | Max.                                    | Unit |
|---------------------------|--|---|---|---|---|------|
| <b>HV Section</b>         |  |   |   |   |   |      |
| I <sub>HV</sub>           | Maximum Supply Current, HV Pin                                 | V <sub>AC</sub> =90 V (V <sub>DC</sub> =120 V),<br>V <sub>DD</sub> =0 V | 1.50                                    | 3.25                                    | 5.00                                    | mA   |
| V <sub>AC-OFF</sub>       | Threshold Voltage for Brownout                                 | DC Source Series<br>R=200 kΩ to HV Pin                                  | 90                                      | 100                                     | 110                                     | V    |
| V <sub>AC-ON</sub>        | Threshold Voltage for Brown-in                                 | DC Source Series<br>R=200 kΩ to HV Pin                                  | 100                                     | 110                                     | 120                                     | V    |
| ΔV <sub>AC</sub>          | V <sub>AC-ON</sub> – V <sub>AC-OFF</sub>                       | DC Source Series<br>R=200 kΩ to HV Pin                                  | 8                                       | 12                                      | 16                                      | V    |
| t <sub>D-AC-OFF</sub>     | Debounce Time for Brownout                                     |   | 40                                      | 65                                      | 90                                      | ms   |
| t <sub>S-WORK</sub>       | Work Period of HV-Sampling<br>Circuit in Deep Burst Mode       | Deep Burst Mode,<br>V <sub>FB</sub> <V <sub>FB-ZDC-DBM</sub>            | 95                                      | 140                                     | 185                                     | ms   |
| t <sub>S-REST</sub>       | Rest Period of HV-Sampling<br>Circuit in Deep Burst Mode       | Deep Burst Mode,<br>V <sub>FB</sub> <V <sub>FB-ZDC-DBM</sub>            | 180                                     | 260                                     | 320                                     | ms   |
| V <sub>HV-DIS</sub>       | X-Cap. Discharge Threshold                                     | R <sub>HV</sub> =200 kΩ to HV Pin                                       | V <sub>DC</sub> <sup>(5)</sup><br>×0.45 | V <sub>DC</sub> <sup>(5)</sup><br>×0.51 | V <sub>DC</sub> <sup>(5)</sup><br>×0.56 | V    |
| t <sub>D-HV-DIS</sub>     | Debounce Time for Triggering<br>X-Cap. Discharge               |   | 75                                      | 115                                     | 155                                     | ms   |
| t <sub>HV-DIS</sub>       | Discharge Time when X-Cap.<br>Discharge is Triggered           |   | 360                                     | 510                                     | 660                                     | ms   |
| <b>Oscillator Section</b> |  |   |   |   |   |      |
| f <sub>OSC</sub>          | Switching Frequency when<br>V <sub>FB</sub> >V <sub>FB-N</sub> | Center Frequency  | 62                                      | 65                                      | 68                                      | kHz  |
|                           |  | Hopping Range   | ±3.55                                   | ±4.25                                   | ±4.95                                   |      |
| t <sub>HOP</sub>          | Hopping Period <sup>(6)</sup>                                  | V <sub>FB</sub> >V <sub>FB-G</sub>                                      | 5.12                                    | 6.40                                    | 7.68                                    | ms   |
| f <sub>OSC-G</sub>        | Switching Frequency when<br>V <sub>FB</sub> <V <sub>FB-G</sub> | V <sub>FB</sub> <V <sub>FB-G</sub>                                      | 20                                      | 23                                      | 26                                      | kHz  |
| f <sub>DV</sub>           | Frequency Variation vs. V <sub>DD</sub><br>Deviation           | V <sub>DD</sub> =11 to 22 V   |   |   | 5                                       | %    |
| f <sub>DT</sub>           | Frequency Variation vs.<br>Temperature Deviation               | T <sub>A</sub> =-40 to 105°C  |   |   | 5                                       | %    |

Continued on the following page...

**Electrical Characteristics** (Continued)V<sub>DD</sub>=15 V and T<sub>J</sub>=T<sub>A</sub>=25°C unless otherwise noted.

| Symbol                        | Parameter  | Condition   | Min.  | Typ.  | Max.  | Unit |
|-------------------------------|--|---|-------|-------|-------|------|
| <b>Feedback Input Section</b> |  |   |       |       |       |      |
| A <sub>V</sub>                | Feedback Voltage to Current-Sense Attenuation                        |   | 1/4.5 | 1/4.0 | 1/3.5 | V/V  |
| Z <sub>FB</sub>               | Regular FB Internal Pull-High Impedance                              |   |       | 8.5   |       | kΩ   |
| V <sub>FB-OPEN</sub>          | FB Internal Biased Voltage   | FB Pin Open   | 5.2   | 5.4   | 5.6   | V    |
| V <sub>FB-OLP</sub>           | Threshold Voltage for OLP  |   | 4.3   | 4.6   | 4.9   | V    |
| t <sub>D-OLP</sub>            | Delay for OLP  |   | 45.0  | 57.5  | 70.0  | ms   |
| V <sub>FB-N</sub>             | Threshold Voltage for Maximum Switching Frequency                    |   | 2.6   | 2.8   | 3.0   | V    |
| V <sub>FB-G</sub>             | Threshold Voltage for Minimum Switching Frequency                    |   | 2.1   | 2.3   | 2.5   | V    |
| V <sub>FB-ZDCR</sub>          | FB Threshold Voltage for Zero-Duty Recovery                          |   | 1.9   | 2.1   | 2.3   | V    |
| V <sub>FB-ZDC</sub>           | FB Threshold Voltage for Zero-Duty                                   |   | 1.8   | 2.0   | 2.2   | V    |
| V <sub>FB-ZDCR-DBM</sub>      | FB Threshold Voltage for Zero-Duty Recovery in Deep Burst Mode       | V <sub>DD</sub> =V <sub>UVLO</sub> +0.3 V                           | 2.5   | 2.7   | 2.9   | V    |
| V <sub>FB-ZDC-DBM</sub>       | FB Threshold Voltage for Zero-Duty in Deep-Burst Mode                |   | 2.35  | 2.55  | 2.75  | V    |
| t <sub>DBM</sub>              | Condition of Triggering Deep Burst Mode                              | V <sub>FB</sub> <V <sub>FB-ZDC</sub> Repeats 3 Times Continuously   |       | 7.5   |       | ms   |
| t <sub>D-DBM</sub>            | Delay time of Entering Deep Burst Mode                               |   | 600   |       |       | ms   |
| V <sub>FB-RECOVER</sub>       | Threshold Voltage for Leaving Deep Burst Mode Immediately            | Deep Burst Mode, V <sub>DD</sub> >V <sub>DD-ZFBR</sub> and Gate Off |       | 0.9   |       | V    |
| <b>Current-Sense Section</b>  |  |   |       |       |       |      |
| t <sub>PD</sub>               | Propagation Delay to Output  |   |       | 100   | 250   | ns   |
| t <sub>LEB</sub>              | Leading Edge Blanking Time   |   | 200   | 265   | 330   | ns   |
| V <sub>LIMIT-L</sub>          | Current Limit at Low Line (V <sub>AC-RMS</sub> =86 V)                | V <sub>DC</sub> =122 V, Series R=200 kΩ to HV                       | 0.43  | 0.46  | 0.49  | V    |
| V <sub>LIMIT-H</sub>          | Current Limit at High Line (V <sub>AC-RMS</sub> =259 V)              | V <sub>DC</sub> =366 V, Series R=200 kΩ to HV                       | 0.36  | 0.39  | 0.42  | V    |
| V <sub>SSCP-L</sub>           | Threshold Voltage for SSCP at Low Line (V <sub>AC-RMS</sub> =86 V)   | V <sub>DC</sub> =122 V, Series R=200 kΩ to HV                       | 30    | 50    | 70    | mV   |
| V <sub>SSCP-H</sub>           | Threshold Voltage for SSCP at High Line (V <sub>AC-RMS</sub> =259 V) | V <sub>DC</sub> =366 V, Series R=200 kΩ to HV                       | 80    | 100   | 120   | mV   |
| t <sub>ON-SSCP</sub>          | Minimum On-time of Gate to Trigger SSCP                              | V <sub>SENSE</sub> <V <sub>SSCP-(L/H)</sub>                         | 4.00  | 4.55  | 5.10  | μs   |
| t <sub>D-SSCP</sub>           | Debounce Time for SSCP   | V <sub>SENSE</sub> <V <sub>SSCP-(L/H)</sub>                         | 110   | 170   | 230   | μs   |
| t <sub>SS</sub>               | Soft-Start Time  | Startup   | 5     | 7     | 9     | ms   |

Continued on the following page...

**Electrical Characteristics** (Continued)V<sub>DD</sub>=15V and T<sub>J</sub>=T<sub>A</sub>=25°C unless otherwise noted.

| Symbol   | Parameter   | Condition   | Min.  | Typ.                 | Max.  | Unit   |
|--|---|---|-------|----------------------|-------|--------|
| <b>GATE Section</b>                              |   |   |       |                      |       |        |
| DCY <sub>MAX</sub>                               | Maximum Duty Cycle  |   | 75.0  | 82.5                 | 90.0  | %      |
| V <sub>GATE-L</sub>                              | Gate Low Voltage  | V <sub>DD</sub> =15 V,<br>I <sub>O</sub> =5 mA                                      |       |                      | 1.5   | V      |
| V <sub>GATE-H</sub>                              | Gate High Voltage   | V <sub>DD</sub> =1 V, I <sub>O</sub> =5 mA  | 8     |                      |       | V      |
| t <sub>r</sub>                                   | Gate Rising Time  | V <sub>DD</sub> =1 V, C <sub>L</sub> = nF   |       | 110                  |       | ns     |
| t <sub>f</sub>                                   | Gate Falling Time   | V <sub>DD</sub> =15 V, C <sub>L</sub> =1 nF   |       | 40                   |       | ns     |
| V <sub>GATE-CLAMP</sub>                          | Gate Output Clamping Voltage  | V <sub>DD</sub> =22 V   | 11.0  | 14.5                 | 18.0  | V      |
| n <sub>SKIP</sub>                                | Continuously Gate Switching Number for Leaving Deep-Burst Mode <sup>(6)</sup> |   |       | 112                  |       | pulses |
| <b>RT Section</b>                                |   |   |       |                      |       |        |
| I <sub>RT</sub>                                  | Output Current of RT Pin  |   |       | 100                  |       | μA     |
| V <sub>RTTH1</sub>                               | Threshold Voltage for Over-Temperature Protection                             | V <sub>RTTH2</sub> < V <sub>RT</sub> < V <sub>RTTH1</sub> , Latch Off After 14.5 ms | 1.000 | 1.035                | 1.070 | V      |
| V <sub>RTTH2</sub>                               | Threshold Voltage for Latch Triggering  | V <sub>RT</sub> < V <sub>RTTH2</sub> , Latch Off After 185 μs                       | 0.65  | 0.70                 | 0.75  | V      |
| R <sub>OTP</sub>                                 | Maximum External Resistance of RT Pin to Trigger Latch Protection             |   | 9.66  | 10.50                | 11.34 | kΩ     |
| t <sub>D-OTP1</sub>                              | Debounce Time for Over-Temperature Protection Triggering                      | V <sub>RTTH2</sub> < V <sub>RT</sub> < V <sub>RTTH1</sub>                           | 11.0  | 14.5                 | 18.0  | ms     |
| t <sub>D-OTP2</sub>                              | Debounce Time for Latch Triggering  | V <sub>RT</sub> < V <sub>RTTH2</sub>  | 110   | 185                  | 260   | μs     |
| <b>Over-Temperature Protection Section (OTP)</b> |   |   |       |                      |       |        |
| T <sub>OTP</sub>                                 | Protection Junction Temperature <sup>(6,7)</sup>                              |   |       | +135                 |       | °C     |
| T <sub>RESTART</sub>                             | Restart Junction Temperature <sup>(6)</sup>                                   |   |       | T <sub>OTP</sub> -25 |       | °C     |

**Notes:**

- V<sub>DC</sub> is V<sub>AC</sub> × √2.
- Guaranteed by design.
- When activated, the output is stopped until junction temperature drops below T<sub>RESTART</sub>.



## Typical Performance Characteristics

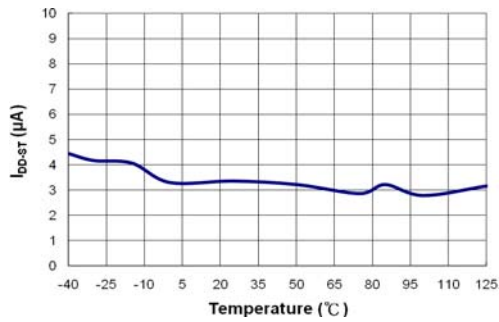


Figure 5. Startup Current ( $I_{DD-ST}$ ) vs. Temperature

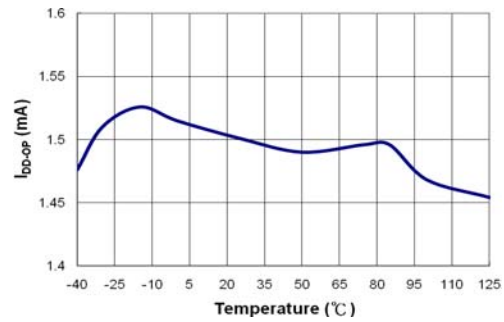


Figure 6. Operation Supply Current ( $I_{DD-OP1}$ ) vs. Temperature

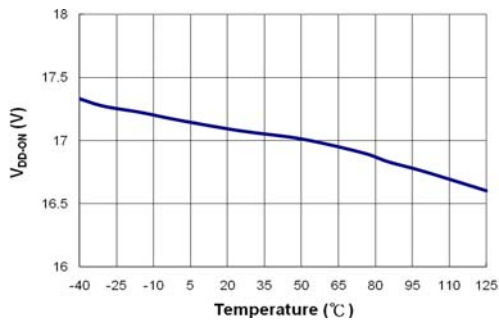


Figure 7. Start Threshold Voltage ( $V_{DD-ON}$ ) vs. Temperature

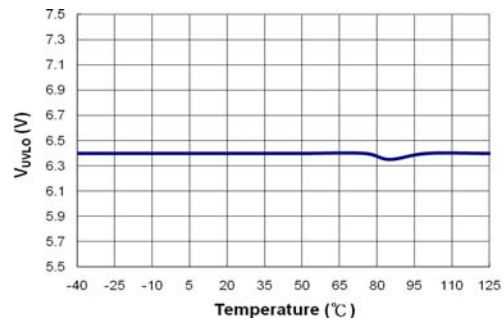


Figure 8. Minimum Operating Voltage ( $V_{UVLO}$ ) vs. Temperature

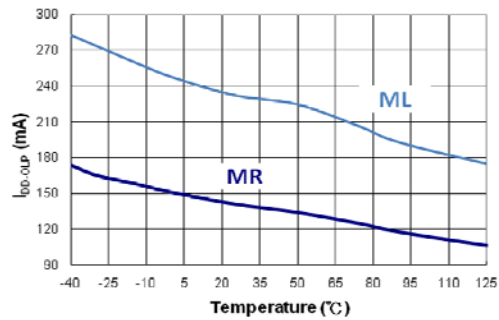


Figure 9. OFF-State Internal Sink Current Under Protection Mode ( $I_{DD-OLP}$ ) vs. Temperature

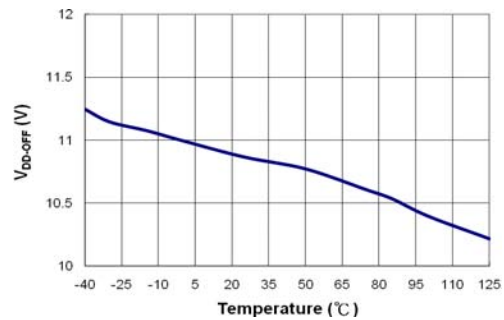


Figure 10. Minimum Operating Voltage Under Protection Mode ( $V_{DD-OFF}$ ) vs. Temperature

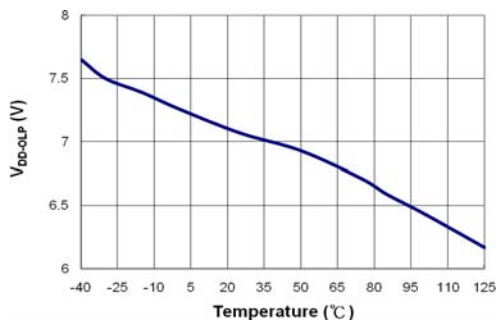


Figure 11. Threshold Voltage to Enable HV startup in Protection Mode ( $V_{DD-OLP}$ ) vs. Temperature

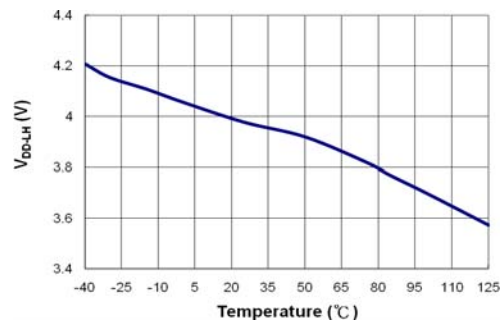
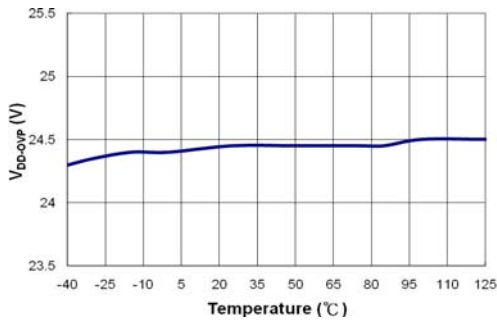
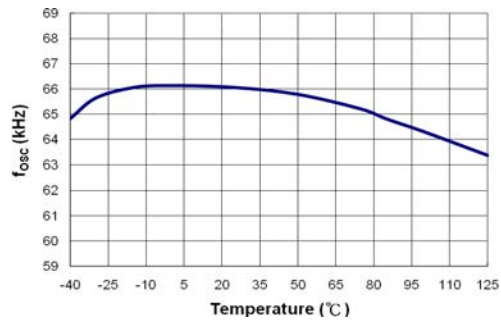


Figure 12. Threshold Voltage to Release Latch Mode ( $V_{DD-LH}$ ) vs. Temperature

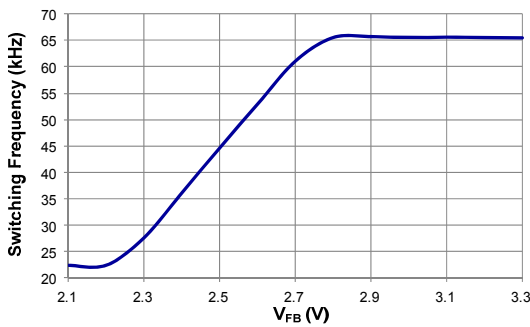
**Typical Performance Characteristics (Continued)**



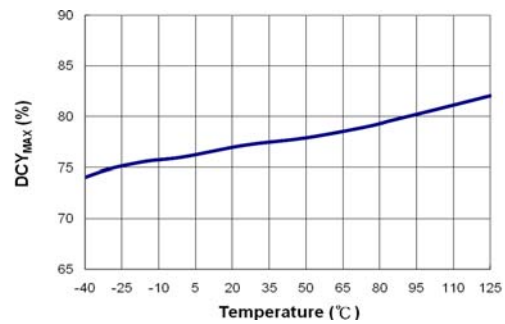
**Figure 13. V<sub>DD</sub> Over-Voltage Protection (V<sub>DD-OVP</sub>) vs. Temperature**



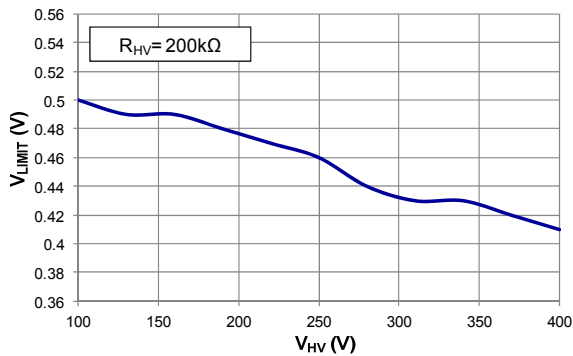
**Figure 14. Frequency in Normal Mode (f<sub>OSC</sub>) vs. Temperature**



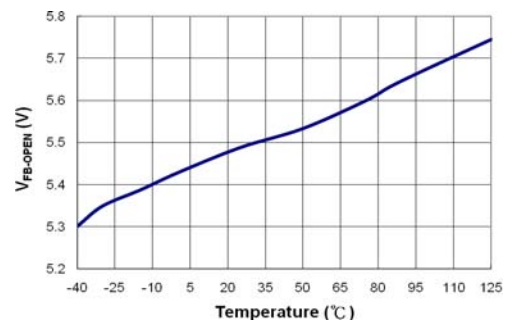
**Figure 15. PWM Switching Frequency vs. Feedback Voltage (V<sub>FB</sub>)**



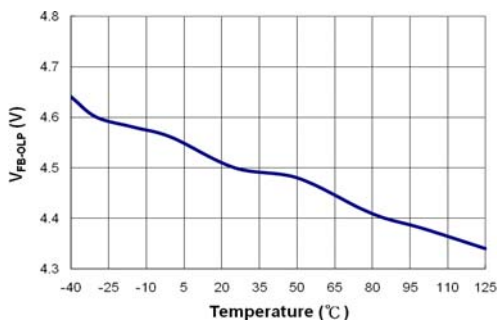
**Figure 16. Maximum Duty Cycle (DCY<sub>MAX</sub>) vs. Temperature**



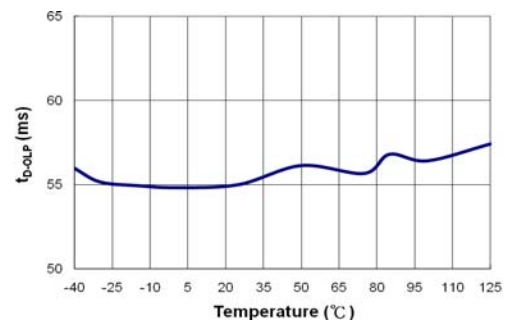
**Figure 17. Current Limit (V<sub>LIMIT</sub>) vs. HV Voltage (V<sub>HV</sub>)**



**Figure 18. FB-Pin Internal Bias Voltage (V<sub>FB-OPEN</sub>) vs. Temperature**

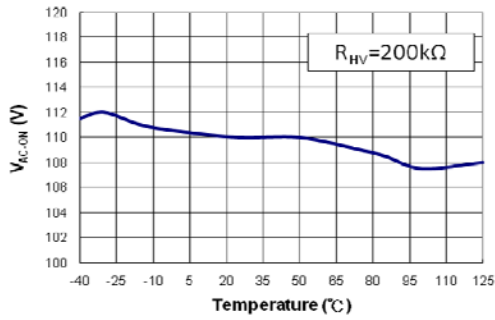


**Figure 19. Open-Loop Protection Triggering Level (V<sub>FB-OLP</sub>) vs. Temperature**

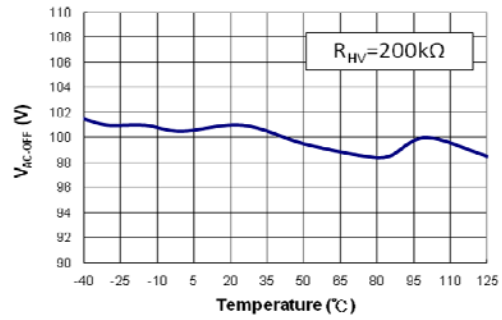


**Figure 20. Delay Time of Open-Loop Protection (t<sub>D-OLP</sub>) vs. Temperature**

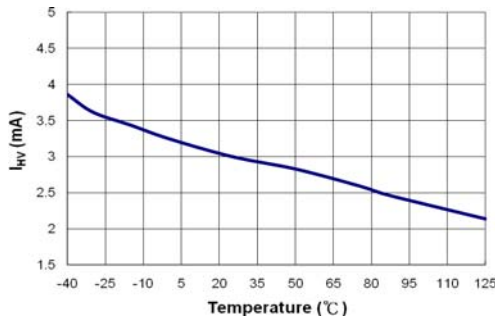
**Typical Performance Characteristics** (Continued)



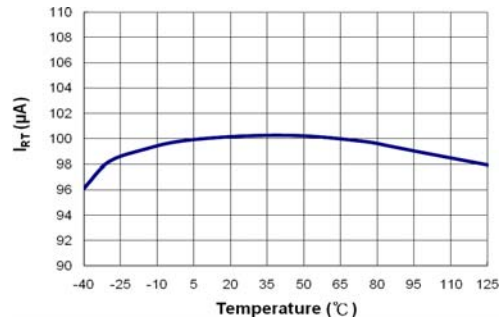
**Figure 21. Brown-in ( $V_{AC-ON}$ ) vs. Temperature**



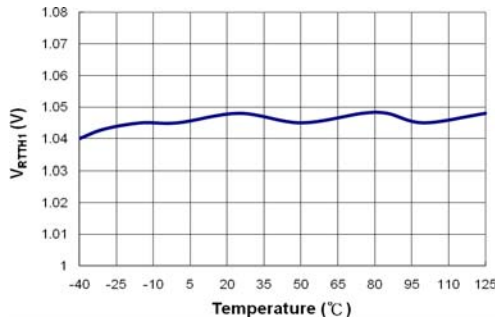
**Figure 22. Brownout ( $V_{AC-OFF}$ ) vs. Temperature**



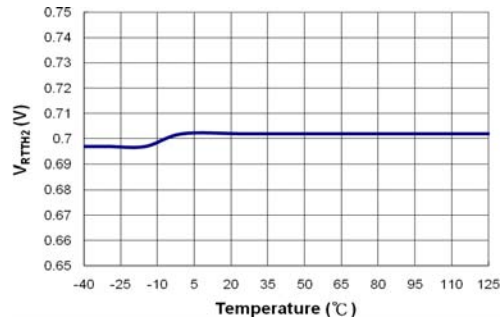
**Figure 23. Inherent Current Limit of HV-Pin ( $I_{HV}$ ) vs. Temperature**



**Figure 24. Output Current from RT Pin ( $I_{RT}$ ) vs. Temperature**



**Figure 25. Over-Temperature Protection Threshold Voltage ( $V_{RTTH1}$ ) vs. Temperature**



**Figure 26. Over-Temperature Protection Threshold Voltage ( $V_{RTTH2}$ ) vs. Temperature**



## Functional Description

### Current Mode Control

FAN6756 employs Peak-Current Mode control, as shown in Figure 27. An opto-coupler (such as the H11A817A) and a shunt regulator (such as the KA431) are typically used to implement the feedback network. Comparing the feedback voltage with the voltage across the  $R_{sense}$  resistor makes it possible to control the switching duty cycle. The built-in slope compensation stabilizes the current loop and prevents sub-harmonic oscillation.

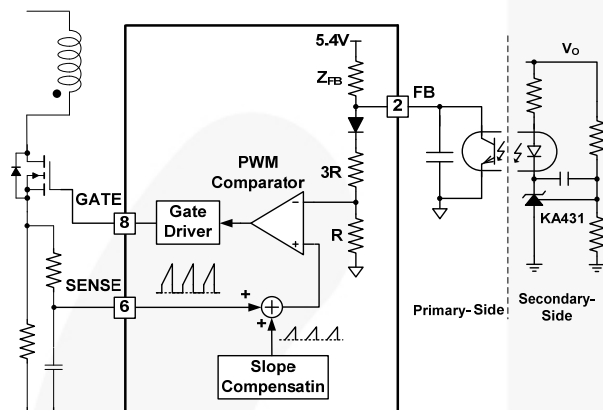


Figure 27. Current-Mode Control Circuit Diagram

### Leading-Edge Blanking (LEB)

Each time the power MOSFET is switched on, a turn-on spike occurs on the sense resistor. To avoid premature termination of the switching pulse, a leading-edge blanking time,  $t_{LEB}$ , is introduced. During this blanking period, the current-limit comparator is disabled and cannot switch off the gate driver.

### mWSaver™ Technology

#### Green-Mode

FAN6756 modulates the PWM frequency as a function of the FB voltage to improve the medium- and light-load efficiency, as shown in Figure 28. Since the output power is proportional to the FB voltage in Current-Mode control, the switching frequency decreases as load decreases. In heavy-load conditions, the switching frequency is fixed at 65 kHz. Once  $V_{FB}$  decreases below  $V_{FB-N}$  (2.8 V), the PWM frequency starts linearly decreasing from 65 kHz to 23 kHz to reduce switching losses. As  $V_{FB}$  drops to  $V_{FB-G}$  (2.3 V), where switching frequency is decreased to 23 kHz, the switching frequency is fixed to avoid acoustic noise.

When  $V_{FB}$  falls below  $V_{FB-ZDC}$  (2.0 V) as load decreases further, the FAN6756 enters Burst Mode, where PWM switching is disabled. Then the output voltage starts to drop, causing the feedback voltage to rise. Once  $V_{FB}$  rises above  $V_{FB-ZDCR}$  (2.1 V), switching resumes. Burst Mode alternately enables and disables switching, thereby reducing switching loss for lower power consumption, as shown in Figure 29.

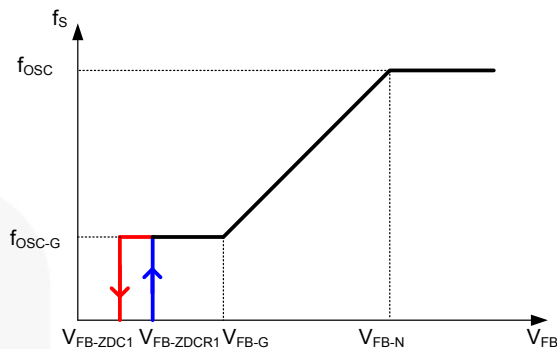


Figure 28.  $V_{FB}$  vs. PWM Frequency

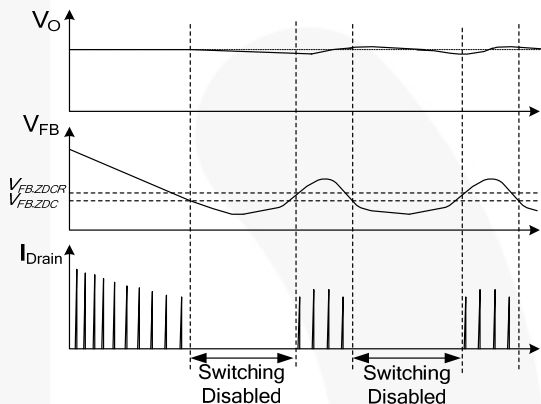


Figure 29. Burst Switching in Green Mode

#### Deep Burst Mode & Feedback Impedance Switching

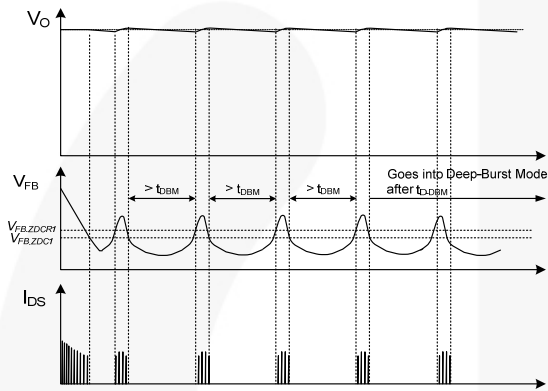
Deep Burst Mode is defined as a special operational mode to minimize power consumption at extremely light-load or no-load condition where, not only the switching loss, but also power consumption of the FAN6756 itself, are reduced further than in Green Mode. Deep Burst Mode is initiated when the non-switching state of burst switching in Green Mode persists longer than  $t_{DBM}$  (7.5 ms) for three consecutive burst switchings (as shown in Figure 30). To prevent entering Deep Burst Mode during dynamic load change, there is  $t_{D-DBM}$  (>600 ms) delay. If there are more than 112 consecutive switching pulses during the  $t_{D-DBM}$  delay, the FAN6756 does not go into Deep Burst Mode.

Once the FAN6756 enters Deep Burst Mode, the feedback impedance,  $Z_{FB}$ , is modulated by the impedance modulator, as shown in Figure 31. When  $V_{FB}$  is under a threshold level, the impedance modulator clamps  $V_{FB}$  and disables switching. When  $V_{DD}$  drops to  $V_{DD-ZFBR}$  (7 V, which is 0.5 V higher than  $V_{UVLO}$ ), the impedance modulator controls  $Z_{FB}$ , allowing  $V_{FB}$  to rise and resume switching operation. As shown in Figure 32, by clamping  $V_{FB}$  to disable switching while modulating  $Z_{FB}$  to enable switching, the system is forced into a “Deep” Burst Mode to reduce switching loss.

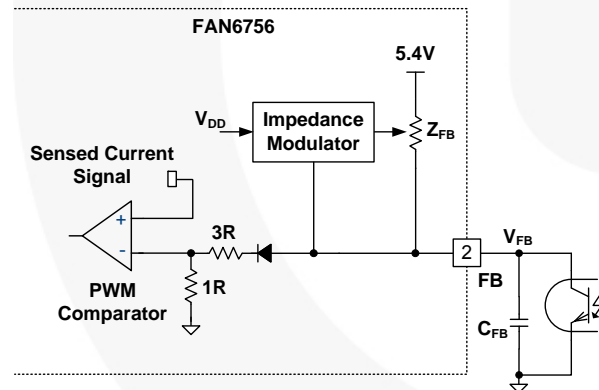
Deep Burst Mode maintains  $V_{DD}$  as low as possible so power consumption can be minimized. When the FAN6756 enters Deep Burst Mode, several blocks are disabled and the operation current is reduced from  $I_{DD-OP1}$  (1.8 mA) to  $I_{DD-OP2}$  (450  $\mu$ A).

The feedback voltage thresholds where FAN6756 enters and exits Burst Mode change from  $V_{FB-ZDC}$  (2.0 V) and  $V_{FB-ZDCR}$  (2.1 V) to  $V_{FB-ZDC-DBM}$  (2.55 V) and  $V_{FB-ZDCR-DBM}$  (2.7 V) in Deep Burst Mode. This reduces the switching loss more by increasing the energy delivered to the load per switching operation, which eventually reduces the total switching for a given load condition.

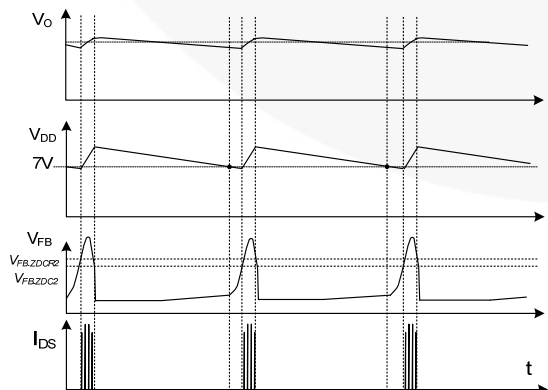
The FAN6756 exits Deep Burst Mode after more than 112 consecutive switching pulses in Deep Burst Mode. Once the FAN6756 exits Deep Burst Mode, the feedback impedance is modulated to 8.5 kΩ to keep the original loop response. The FAN6756 also exits Deep Burst Mode when the opto-coupler transistor current is virtually zero and  $V_{FB}$  rises above  $V_{FB-RECOVER}$  (0.9 V) while switching is suspended.



**Figure 30. Entering Deep Burst Mode**



**Figure 31. Feedback Impedance Modulation**

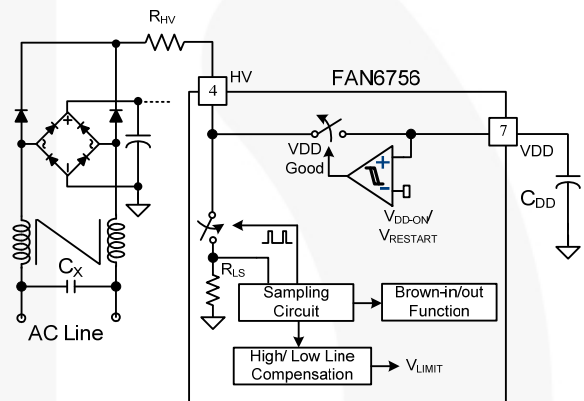


**Figure 32. Operation in Deep Burst Mode**

### High-Voltage Startup and Line Sensing

The HV pin is typically connected to the AC line input through two external diodes and one resistor ( $R_{HV}$ ), as shown in Figure 33. When the AC line voltage is applied, the  $V_{DD}$  hold-up capacitor is charged by the line voltage through the diodes and resistor. After  $V_{DD}$  voltage reaches the turn-on threshold voltage ( $V_{DD-ON}$ ), the startup circuit charging the  $V_{DD}$  capacitor is switched off and  $V_{DD}$  is supplied by the auxiliary winding of the transformer. Once the FAN6756 starts, it continues operating until  $V_{DD}$  drops below 6.5 V ( $V_{UVLO}$ ). IC startup time with a given AC line input voltage is given as:

$$t_{STARTUP} = R_{HV} \cdot C_{DD} \cdot \ln \frac{V_{AC-IN} \cdot \frac{2\sqrt{2}}{\pi}}{V_{AC-IN} \cdot \frac{2\sqrt{2}}{\pi} - V_{DD-ON}} \quad (1)$$



**Figure 33. Startup Circuit**

The HV pin detects the AC line voltage using a switched voltage divider that consists of external resistor ( $R_{HV}$ ) and internal resistor ( $R_{LS}$ ), as shown in Figure 33. The internal line-sensing circuit detects line voltage using a sampling circuit and peak-detection circuit. Since the voltage divider causes power consumption when it is switched on, the switching is driven by a signal with a very narrow pulse width to minimize power loss. The sampling frequency is adaptively changed according to the load condition to minimize power consumption in light-load condition.

Based on the detected line voltage, brown-in and brownout thresholds are determined as:

$$V_{BROWN-IN} (RMS) = \frac{R_{HV}}{200k} \cdot \frac{V_{AC-ON}}{\sqrt{2}} \quad (2)$$

$$V_{BROWNOUT} (RMS) = \frac{R_{HV}}{200k} \cdot \frac{V_{AC-OFF}}{\sqrt{2}} \quad (3)$$

Since the internal resistor ( $R_{LS}=1.6$  kΩ) of the voltage divider is much smaller than  $R_{HV}$ , the thresholds are given as a function of  $R_{HV}$ .

#### Note:

- $V_{DD}$  must be larger than  $V_{DD-AC}$  to start, even though the sensed line voltage satisfies Equation (2), as shown in Figure 34.



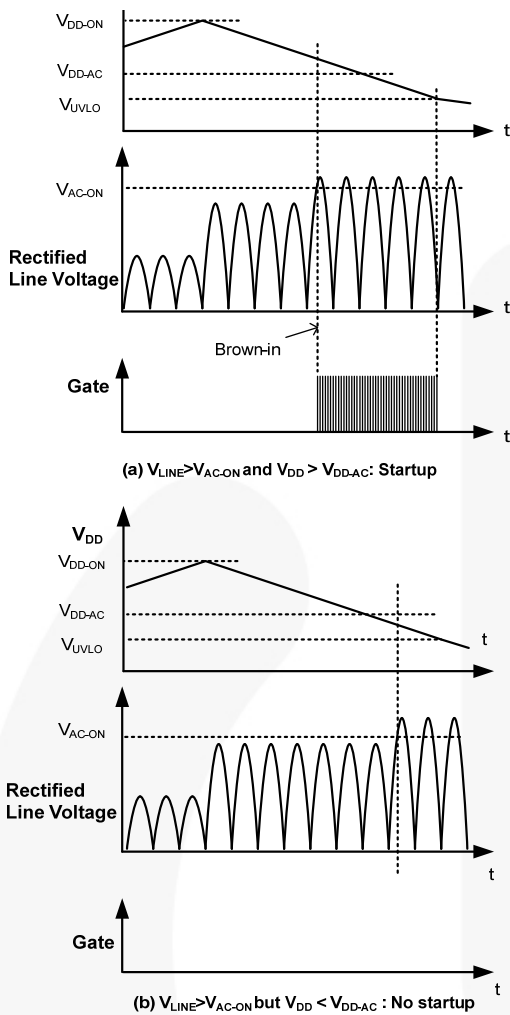


Figure 34. Timing Diagram for Brown-in Function

**AX-CAP® Discharge**

The EMI filter in the front end of the switched-mode power supply (SMPS) typically includes a capacitor across the AC line connector (C<sub>X</sub>). Most of the safety regulations, such as UL 1950 and IEC61010-1, require that the capacitor be discharged to a safe level within a given time when the AC plug is abruptly removed from its receptacle. Typically, discharge resistors across the capacitor are used to make sure that capacitor is discharged naturally, which introduces power loss as long as it is connected to the receptacle.

Fairchild's innovative AX-CAP® technology intelligently discharges the filter capacitor only when the power supply is unplugged from the power outlet. Since the discharging circuit is disabled in normal operation, the power loss in the EMI filter can be virtually removed.

The discharge of the capacitor is achieved through the HV pin. Once AC outlet detaching is detected, the HV pin behaves as a resistor to ground, so the charges on the capacitor can be discharged through the R<sub>HV</sub> in series with the internal resistor of the HV pin. Since the HV-pin internal resistor is much smaller than R<sub>HV</sub>, the time constant of discharging process is almost R<sub>HV</sub>•C<sub>X</sub>.

**High / Low Line Compensation for Constant Power Limit**

FAN6756 has pulse-by-pulse current limit as shown in Figure 35, which limits the maximum input power with a given input voltage. If the output consumes beyond this maximum power, the output voltage drops, triggering the overload protection.

As shown in Figure 35, based on the line voltage, V<sub>LINE</sub><sup>PK</sup>, the high/low line compensation block adjusts the current limit level, V<sub>LIMIT</sub>, defined as:

$$V_{LIMIT} = \frac{V_{LIMIT-H} - V_{LIMIT-L}}{2} \cdot \frac{R_{LS}}{R_{HV}} \cdot V_{LINE}^{PK} + \frac{3 \cdot V_{LIMIT-L} - V_{LIMIT-H}}{2} \quad (4)$$

To maintain the constant output power limit regardless of line voltage, the cycle-by-cycle current limit level, V<sub>LIMIT</sub>, decreases as line voltage increases. The current limit level is proportional to the R<sub>HV</sub> resistor value and power limit can be tuned using the R<sub>HV</sub> resistor. Figure 36 shows how the pulse-by-pulse current limit changes with the line voltage for different R<sub>HV</sub> resistors.

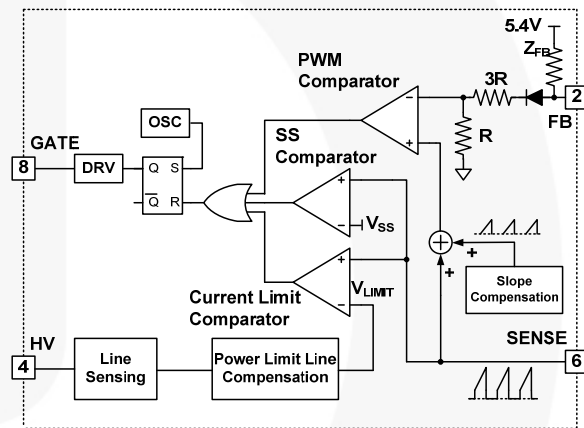


Figure 35. Pulse-by-Pulse Current Limit Circuit

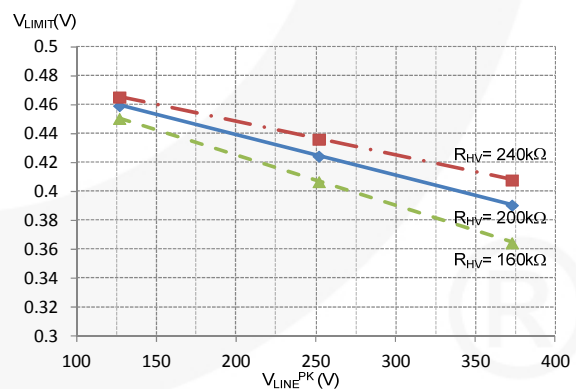


Figure 36. Current Limit vs. Line Voltage

**Soft-Start**

An internal soft-start circuit progressively increases the pulse-by-pulse current-limit level of MOSFET for 7 ms during startup to establish the correct working conditions for transformers and capacitors.

## Protections

FAN6756 provides full protection functions, including Overload / Open-Loop Protection (OLP),  $V_{DD}$  Over-Voltage Protection (OVP), Over-Temperature Protection (OTP), and Current-Sense Short-Circuit Protection (SSCP). SSCP is implemented as Auto-Restart Mode, while OVP and OTP are implemented as Latch Mode protections. OLP is Auto-Restart Mode for FAN6756MRMY and Latch Mode for FAN6756MLMY.

When an Auto-Restart Mode protection is triggered, switching is terminated and the MOSFET remains off, causing  $V_{DD}$  to drop. When  $V_{DD}$  drops to the  $V_{DD-OFF}$  (11 V), the protection is reset. When  $V_{DD}$  drops further to  $V_{DD-OLP}$  (7 V), the internal startup circuit is enabled and the supply current drawn from HV pin charges the hold-up capacitor. When  $V_{DD}$  reaches the turn-on voltage of 17 V, normal operation resumes. In this manner, auto restart alternately enables and disables the MOSFET switching until the abnormal condition is eliminated.

When a Latch Mode protection is triggered, PWM switching is terminated and the MOSFET remains off, causing  $V_{DD}$  to drop. When  $V_{DD}$  drops to the  $V_{DD-OLP}$  (7 V), the internal startup circuit is enabled without resetting the protection and the supply current drawn from HV pin charges the hold-up capacitor. Since the protection is not reset, the IC does not resume PWM switching even when  $V_{DD}$  reaches the turn-on voltage of 17 V, disabling HV startup circuit. Then  $V_{DD}$  drops again down to 7 V. In this manner, the Latch Mode protection alternately charges and discharges  $V_{DD}$  until there is no more energy delivered into HV pin. The protection is reset when  $V_{DD}$  drops to 4 V, which is allowed only after power supply is unplugged from the AC line.

### $V_{DD}$ Over-Voltage Protection (OVP)

$V_{DD}$  over-voltage protection prevents IC damage from voltage exceeding the IC voltage rating. When the  $V_{DD}$  voltage exceeds 24.5 V, the protection is triggered. This protection is typically caused by an open circuit in the secondary-side feedback network.

### Over-Temperature Protection (OTP) and External Latch Triggering

The RT pin provides adjustable Over-Temperature Protection (OTP) and external latch triggering function. For OTP, an NTC thermistor,  $R_{NTC}$ , usually in series with a resistor  $R_A$ , is connected between the RT pin and ground. The internal current source,  $I_{RT}$  (100  $\mu$ A), introduces voltage on RT as:

$$V_{RT} = I_{RT} \cdot (R_{NTC} + R_A) \quad (5)$$

At high ambient temperature,  $R_{NTC}$  decreases, reducing  $V_{RT}$ . When  $V_{RT}$  is lower than  $V_{RTTH1}$  (1.035 V) for longer than  $t_{D-OTP1}$  (14.5 ms), the protection is triggered and the FAN6756 enters Latch Mode protection.

The OTP can be triggered by pulling down the RT pin voltage using an opto-coupler or transistor. Once  $V_{RT}$  is less than  $V_{RTTH2}$  (0.7 V) for longer than  $t_{D-OTP2}$  (185  $\mu$ s), the protection is triggered and the FAN6756 enters Latch Mode protection.

When OTP is not used, place a 100 k $\Omega$  resistor between this pin and ground to prevent noise interference.

### Open-Loop / Overload Protection (OLP)

Because of the pulse-by-pulse current-limit capability, the maximum peak current is limited and, therefore, the maximum input power is also limited. If the output consumes more than this limited maximum power, the output voltage ( $V_O$ ) drops below the set voltage. Then the currents through the opto-coupler and transistor become virtually zero and  $V_{FB}$  is pulled HIGH. Once  $V_{FB}$  is higher than  $V_{FB-OLP}$  (4.6 V) for longer than  $t_{D-OLP}$  (57.5 ms), OLP is triggered. OLP is also triggered when the feedback loop is open by soldering defect.

### Sense Short-Circuit Protection (SSCP)

The FAN6756 provides safety protection for Limited Power Source (LPS) test. When the current-sense resistor is short circuited by a soldering defect during production, current-sensing information is not properly obtained, resulting in unstable power supply operation.

To protect the power supply against a short circuit across the current-sense resistor, FAN6756 shuts down when current sense voltage is very low; even with a relatively large duty cycle. As shown in Figure 37, the current-sense voltage is sampled  $t_{ON-SSCP}$  (4.55  $\mu$ s) after the gate turn-on. If the sampled voltage ( $V_{S-CS}$ ) is lower than  $V_{SSCP}$  for 11 consecutive switching cycles (170  $\mu$ s), the FAN6756 shuts down immediately.  $V_{SSCP}$  varies linearly with line voltage. At 122 V DC input, it is typically 50 mV ( $V_{SSCP-L}$ ); at 366 V DC, it is typically 100 mV ( $V_{SSCP-H}$ ).

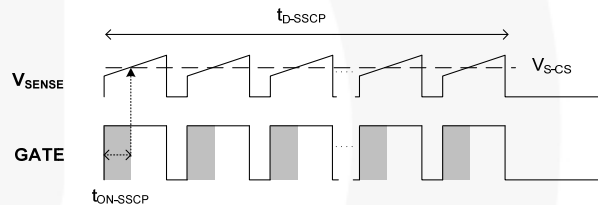


Figure 37. Timing Diagram of SSCP

### Two-Level Under-Voltage Lockout (UVLO)

As shown in Figure 38, as long as protection is not triggered, the turn-off threshold of  $V_{DD}$  is fixed internally at  $V_{UVLO}$  (6.5 V). When a protection is triggered, the  $V_{DD}$  level to terminate PWM gate switching is changed to  $V_{DD-OFF}$  (11 V), as shown in Figure 39. When  $V_{DD}$  drops below  $V_{DD-OFF}$ , the switching is terminated and the operating current from  $V_{DD}$  is reduced to  $I_{DD-OLP}$  to slow down the discharge of  $V_{DD}$  until  $V_{DD}$  reaches  $V_{DD-OLP}$ . This delays re-startup after shutdown by protection to minimize the input power and voltage / current stress of switching devices during a fault condition.

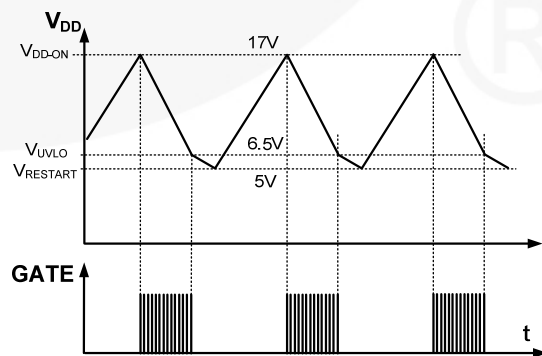


Figure 38.  $V_{DD}$  UVLO at Normal Mode

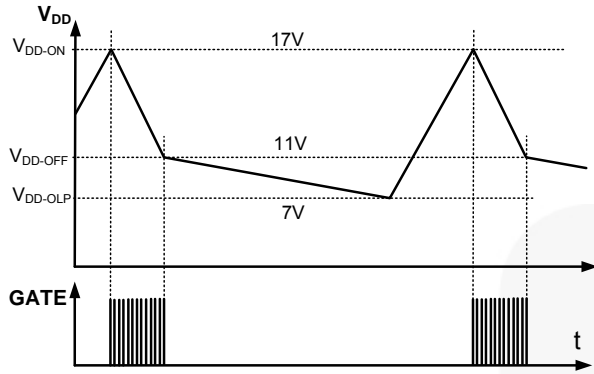


Figure 39.  $V_{DD}$  UVLO at Protection Mode

### Gate Output / Soft Driving

The BiCMOS output stage has a fast totem-pole gate driver. The output driver is clamped by an internal 14.5 V Zener diode to protect the power MOSFET gate from over voltage. A soft driving is implemented to minimize Electromagnetic Interference (EMI) by reducing the switching noise.

### Typical Application Circuit

| Application           | PWM Controller | Input Voltage Range                      | Output       |
|-----------------------|----------------|--|--------------|
| 65 W Notebook Adapter | FAN6756MRMY    | 85 V <sub>AC</sub> ~ 265 V <sub>AC</sub> | 19 V, 3.42 A |

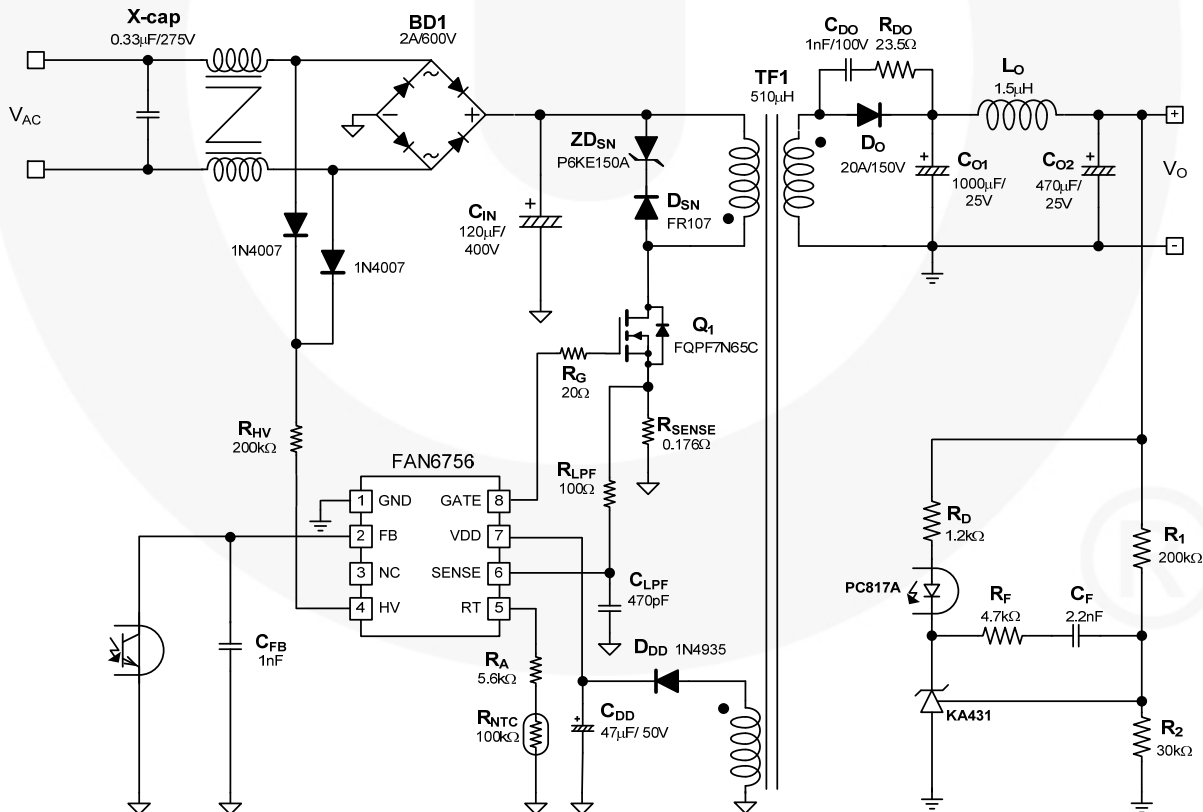


Figure 40. Schematic of Typical Application Circuit



### Transformer Schematic Diagram

- Core: Ferrite Core RM-10
- Bobbin: RM-10

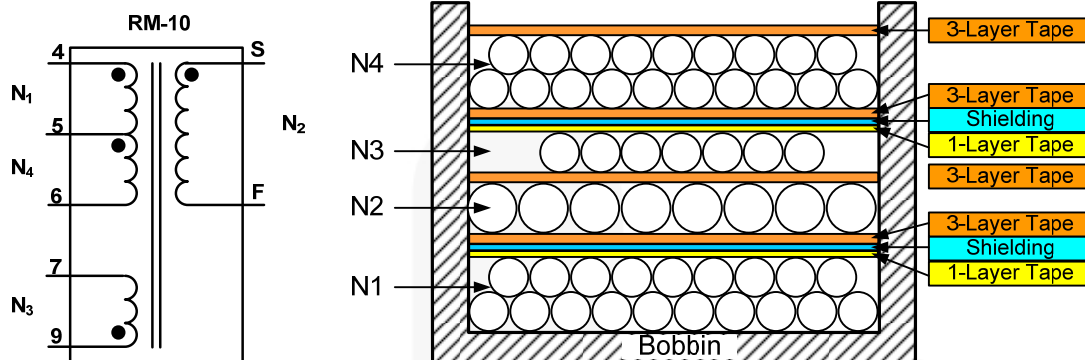


Figure 41. Transformer Specification

### Winding Specification

|   | Pin (Start --> Finish) | Wire   | Turns | Winding Method   | Remark                |
|---|------------------------|--------|-------|------------------|-----------------------|
| N1  | 4 → 5                  | 0.5φ×1 | 19    | Solenoid Winding | Enameled Copper Wire  |
| Insulation: Polyester Tape, t = 0.025 mm, 1-Layer   |                        |        |       |                  |                       |
| Shielding: Adhesive Tape of Copper Foil, t = 0.025×7 mm, 1.2-Layer Open Loop, Connected to Pin 4. |                        |        |       |                  |                       |
| Insulation: Polyester Tape t = 0.025 mm, 3-Layer  |                        |        |       |                  |                       |
| N2  | S → F                  | 0.9φ×1 | 8     | Solenoid Winding | Triple Insulated Wire |
| Insulation: Polyester Tape, t = 0.025 mm, 3-Layer   |                        |        |       |                  |                       |
| N3  | 9 → 7                  | 0.4φ×1 | 7     | Solenoid Winding | Enameled Copper Wire  |
| Insulation: Polyester Tape, t = 0.025 mm, 1-Layer   |                        |        |       |                  |                       |
| Shielding: Adhesive Tape of Copper Foil, t = 0.025×7mm, 1.2-Layer Open Loop, Connected to Pin 4.  |                        |        |       |                  |                       |
| Insulation: Polyester Tape t = 0.025 mm, 3-Layer  |                        |        |       |                  |                       |
| N4  | 5 → 6                  | 0.5φ×1 | 19    | Solenoid Winding | Enameled Copper Wire  |
| Insulation: Polyester Tape t = 0.025 mm, 3-Layer  |                        |        |       |                  |                       |

### Electrical Characteristics

|   | Pin   | Specification | Remark               |
|---|-------|---------------|----------------------|
| Primary-Side Inductance                   | 4 – 6 | 510 μH ±5%    | 1 kHz, 1 V           |
| Primary-Side Effective Leakage Inductance | 4 – 6 | 20 μH Maximum | Short All Other Pins |

### Typical Performance

#### Power Consumption

| Input Voltage       | Output Power | Actual Output Power | Input Power | Specification        |
|---------------------|--------------|---------------------|-------------|----------------------|
| 230 V <sub>AC</sub> | No Load      | 0 W                 | 0.024 W     | Input Power < 0.03 W |
|                     | 0.25 W       | 0.232 W             | 0.339 W     | Input Power < 0.5 W  |
|                     | 0.5 W        | 0.495 W             | 0.643 W     | Input Power < 1 W    |

#### Efficiency

| Output Power | 16.25 W | 32.5 W | 48.75 W | 65 W   | Average |
|--------------|---------|--------|---------|--------|---------|
| 115 V, 60 Hz | 88.48%  | 88.58% | 87.45%  | 86.22% | 87.68%  |
| 230 V, 60 Hz | 88.00%  | 87.89% | 87.92%  | 87.47% | 87.82%  |

Physical Dimensions

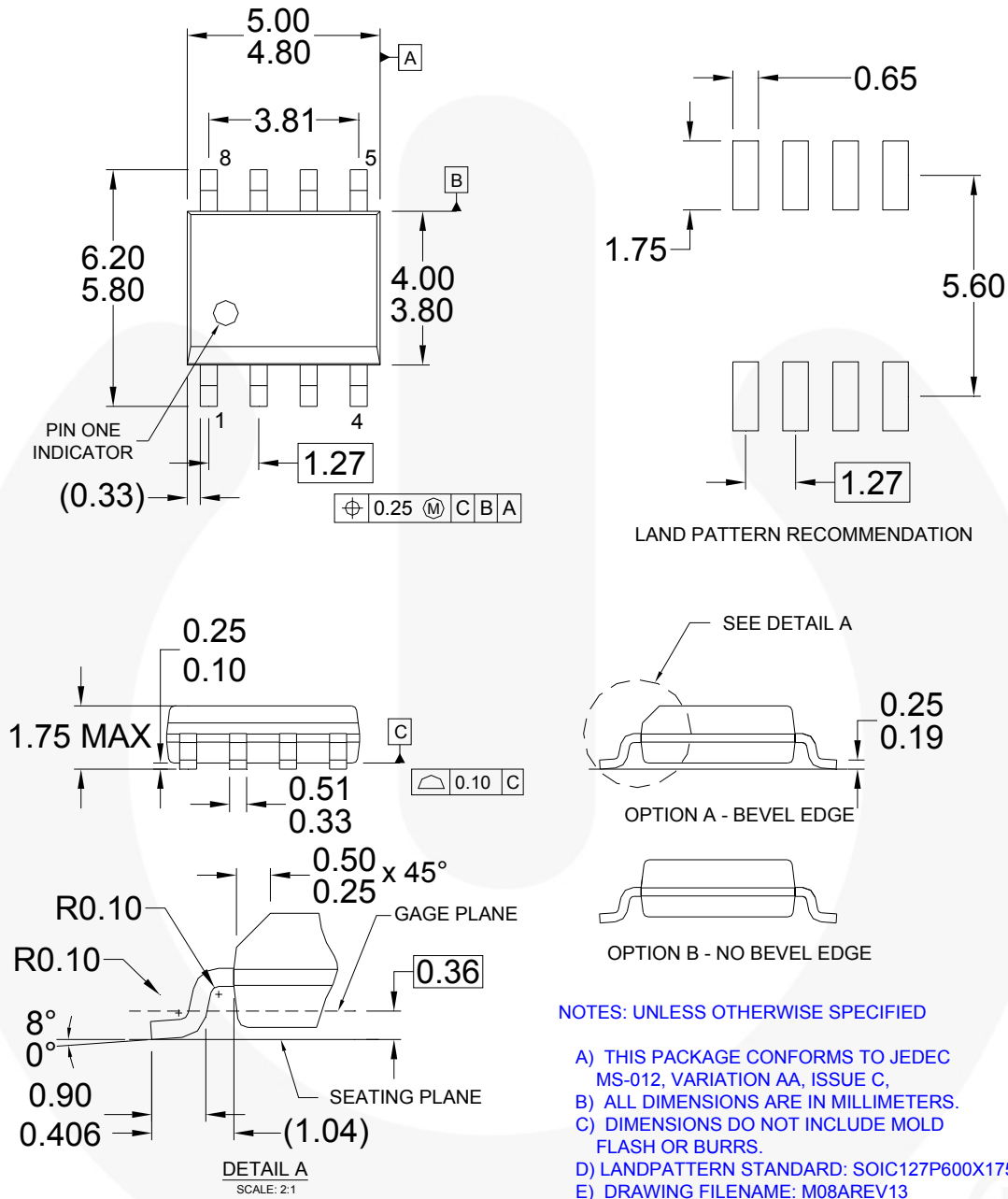


Figure 42. 8-Pin SOP-8 Package

Package drawings are provided as a service to customers considering our components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact our representative to verify or obtain the most recent revision. Package specifications do not expand the terms of our worldwide terms and conditions, specifically the warranty therein, which covers our products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:  
<http://www.fairchildsemi.com/packaging/>



**TRADEMARKS**

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

- |                          |  |                                       |                  |
|--------------------------|--|---------------------------------------|------------------|
| 2Cool™                   | FPS™   |                                       | Sync-Lock™       |
| AccuPower™               | F-PFST™  |                                       |                  |
| AX-CAP®*                 | FRFET®   | PowerTrench®                          | TinyBoost™       |
| BitSiC™                  | Global Power Resource™                         | PowerXS™                              | TinyBuck™        |
| Build it Now™            | GreenBridge™                                   | Programmable Active Droop™            | TinyCalc™        |
| CorePLUS™                | Green FPS™                                     | QFET®                                 | TinyLogic®       |
| CorePOWER™               | Green FPS™ e-Series™                           | QST™                                  | TINYOPTO™        |
| CROSSVOLT™               | Gmax™  | Quiet Series™                         | TinyPower™       |
| CTL™                     | GTO™   | RapidConfigure™                       | TinyPWM™         |
| Current Transfer Logic™  | IntelliMAX™                                    |                                       | TinyWire™        |
| DEUXPEED®                | ISOPLANAR™                                     | Saving our world, 1mW/W/KW at a time™ | TranSiC™         |
| Dual Cool™               | Making Small Speakers Sound Louder and Better™ | SignalWise™                           | TriFault Detect™ |
| EcoSPARK®                | MegaBuck™                                      | SmartMax™                             | TRUECURRENT®*    |
| EfficientMax™            | MICROCOUPLER™                                  | SMART START™                          | µSerDes™         |
| ESBC™                    | MicroFET™                                      | Solutions for Your Success™           |                  |
|                          | MicroPak™                                      | SPM®                                  | UHC®             |
| Fairchild®               | MicroPak2™                                     | STEALTH™                              | Ultra FRFET™     |
| Fairchild Semiconductor® | MillerDrive™                                   | SuperFET®                             | UniFET™          |
| FACT Quiet Series™       | MotionMax™                                     | SuperSOT™-3                           | VCX™             |
| FACT®                    | mWSaver™                                       | SuperSOT™-6                           | VisualMax™       |
| FAST®                    | OptoHiT™                                       | SuperSOT™-8                           | VoltagePlus™     |
| FastvCore™               | OPTOLOGIC®                                     | SupreMOS®                             | XST™             |
| FETBench™                | OPTOPLANAR®                                    | SyncFET™                              |                  |

\* Trademarks of System General Corporation, used under license by Fairchild Semiconductor.

**DISCLAIMER**

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN, NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

**LIFE SUPPORT POLICY**

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

**ANTI-COUNTERFEITING POLICY**

Fairchild Semiconductor Corporation's Anti-Counterfeiting Policy. Fairchild's Anti-Counterfeiting Policy is also stated on our external website, [www.fairchildsemi.com](http://www.fairchildsemi.com), under Sales Support.

Counterfeiting of semiconductor parts is a growing problem in the industry. All manufacturers of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed applications, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handling and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address any warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

**PRODUCT STATUS DEFINITIONS**

**Definition of Terms**

| Datasheet Identification | Product Status        | Definition  |
|--------------------------|-----------------------|---|
| Advance Information      | Formative / In Design | Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.   |
| Preliminary              | First Production      | Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design. |
| No Identification Needed | Full Production       | Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.   |
| Obsolete                 | Not In Production     | Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.  |

Rev. I64

# Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[Fairchild Semiconductor:](#)

[FAN6756MLMY](#) [FAN6756MRMY](#) [FAN6756AMRMY](#) [FAN6756AMLMY](#)