Monolithic Digital AM/FM Receiver Radio-on-a-Chip™

KT0933

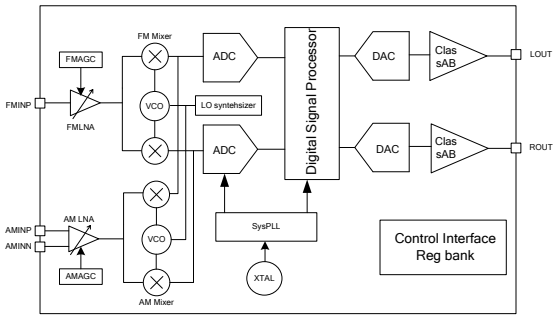
Features

Worldwide full band FM/AM support
FM: 32MHz-110MHz
AM: 500KHz-1750KHz
Fully integrated frequency synthesizer with no external components
High Sensitivity
1.6uVEMF for FM
16uVEMF for AM
High Fidelity
SNR (FM/AM): 60dB/55dB(without weighting filter)
THD: 0.3%
Low Supply Current
28mA (operating)
<45uA (standby)
Advanced features
Automatic antenna tuning
Adjustable AM channel filters (1/2/3/4/5KHz)
Enhanced FM Automatic Frequency Control (AFC) Capability (up to 200KHz)
Flexible Automatic Gain Control (AGC)
Embedded AM/FM SNR meter
Embedded ST indicator
Integrated stereo headphone driver
I^2C control interface for MCU
Advanced Softmute
Flexible stereo Blend
Low supply voltage
2.1V to 3.6V, can be supplied by 2 AAA batteries
Support both 32.768KHz and 38KHz crystal
True Continuous Reference Clock supported
From 30KHz to 40MHz with 3V voltage tolerance
Compatible with EN55020
Small form factor SSOP16L package
RoHS Compliant

Applications

Desktop and portable radio, mini/portable audio systems, clock radio, campus radio, PMP docking station, car audio system, toy and gift.

Rev. 1.3



KT0933 System Diagram

Description

The KT0933 is KT Micro's 3rd generation of proprietary fully integrated AM/FM receiver chip that upgrades the performance, improve the user experience and ease integration and manufacturing efforts. The new features include improved flatness of sensitivity on the whole band, independent status indicator, improved EMI/EMC and higher FM stereo separation.

Thanks to the patented tuning technology, the receiver maintains good signal reception even with short antennas. The chip consumes merely 28mA current and can be powered by 2 AAA batteries. Another useful feature is that the volume and channel information can be preserved in standby mode without external memories. KT0933 supports a wide range of reference clocks from 30KHz to 40MHz, hence can share system clocks with a varieties of MCUs further reducing the system BOM cost. The KT0933 have different user interface schemes like other parts in the KT093x family,

With high audio performance, fully integrated features and low BOM cost, KT0933 is ideal for various applications and products that require flexible programmability for rich features.

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1. Electrical Specification

Table 1: Operation Condition

Parameter	Symbol	Operating Condition	Min	Typ	Max	Units
Power Supply	AVDD	Relative to AVSS	2.1	3.3	3.6	V
Ambient Temperature	Ta		-30	25	70	℃

Table 2: DC Characteristics

Parameter		Symbol	Test/Operating Condition	Min	Typ	Max	Units
Current Consumption	FM Mode	I_{FM}		-	-	30	mA
	AM Mode	I_{AM}		-	-	29	mA
Standby Current		I_{APD}		-	-	45	μA

Table 3: FM Receiver Characteristics

(Unless otherwise noted Ta = -30~70℃, VDD= 2.1V to 3.6V)

Parameter	Symbol	Test/Operating Condition	Min	Typ	Max	Units
FM Frequency Range	F_{rx}		32		110	MHz
Sensitivity[1,2,3]	Sen	(S+N)/N=26dB		1.6	2	uVEMF
Input referred 3rd Order Intermodulation Point[4,5]	IIP3			100		dBuVEMF
Adjacent Channel Selectivity		±200KHz	40		51	dB
Alternate Channel Selectivity		±400KHz	50		70	dB
Image Rejection Radio				43		dB
AM suppression				50		dB
RCLK frequency Range			30	32.768	40,000	KHz
RCLK frequency tolerance[8]			-100		100	ppm
Audio Output Voltage[1,2,3,4]		32ohm load	-	190	-	mV_{RMS}
Audio Band Limits[1,2,4]		±3dB	30		15k	Hz
Audio Stereo Separation [1,4,6]			40			dB
Audio Mono S/N[1,2,3,4]		without weighting filter	55	58		dB
Audio Stereo S/N[1,4,6,7]		DBLND=1 without weighting filter		64		dB
Audio THD[1,2,4,6]				0.3		%
De-emphasis Time Constant		DE=0		75		μs
		DE=1		50		μs
Audio Common Mode Voltage range			0.85	1.35	1.6	V
Audio Output Load Resistance	R_L	Single-ended		32		Ω
Tune Time					50	ms
Power-up Time			200		600	ms

Notes:
1. FMOD=1KHz, 75us de-emphasis
2. MONO=1
3. △F=22.5KHz
4. V_{EMF}=1mV, Frx=32MHz~110MHz

5. RFAGCD=1
6. △F=75KHz
7. VOLUME<4:0>=11111
8. The supported RCLK frequency is continuous. Please refer to application notes.

Table 4: AM Receiver Characteristics

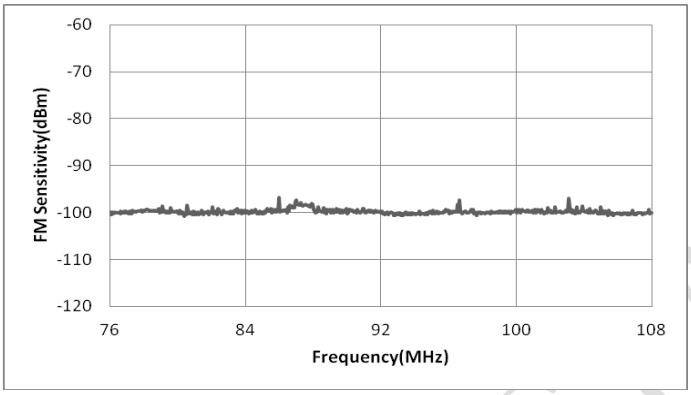
(Unless otherwise noted Ta = -30~70℃, VDD= 2.1V to 3.6V)

Parameter	Symbol	Test/Operating Condition	Min	Typ	Max	Units
AM Frequency Range	F_{rx}		500		1750	KHz
Sensitivity[1,2]	Sen	(S+N)/N=26dB		15		uVEMF
Audio Output Voltage[1,2,3,4]		32ohm load		190		mV_{RMS}
Audio Mono S/N[1,2,3,4]				55		dB
Audio THD[1,2,4]				0.3	0.6	%
Antenna inductance	L		360	-	620	uH

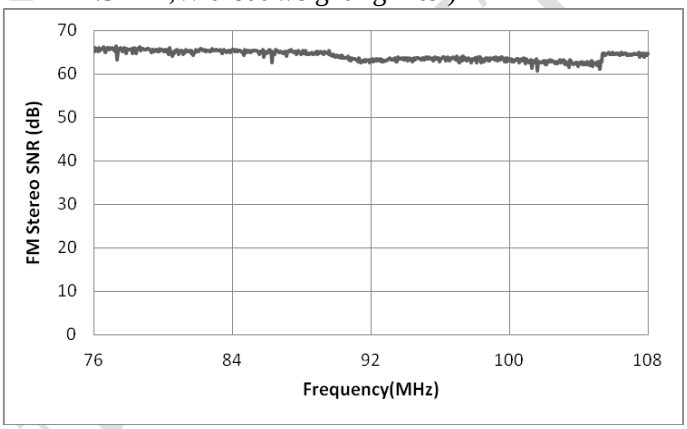
Notes:
1. FMOD=1KHz
2. Modulation index is 30%
3. V_{EMF}=1mV, Frx=500KHz~1750KHz
4. VOLUME<4:0>=11111

2. Typical performance characteristics

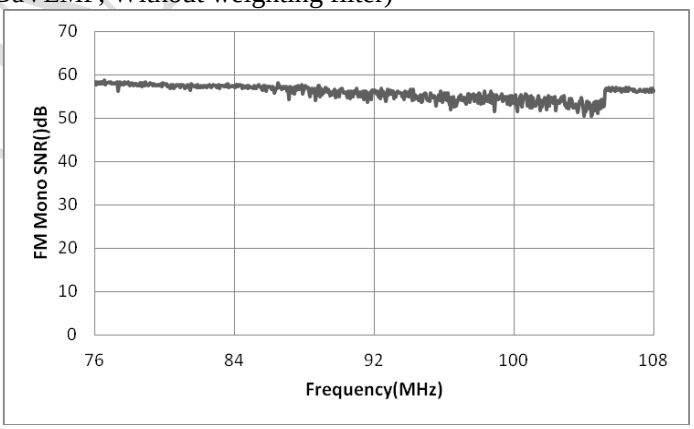
2.1. FM Characteristics



Test condition (Ta = 27℃, VDD= 3.0V, Crystal=32.768KHz, SNR=40dB, FMOD=1KHz, 75us de-emphasis,MONO=1, △F=22.5KHz,Without weighting filter)

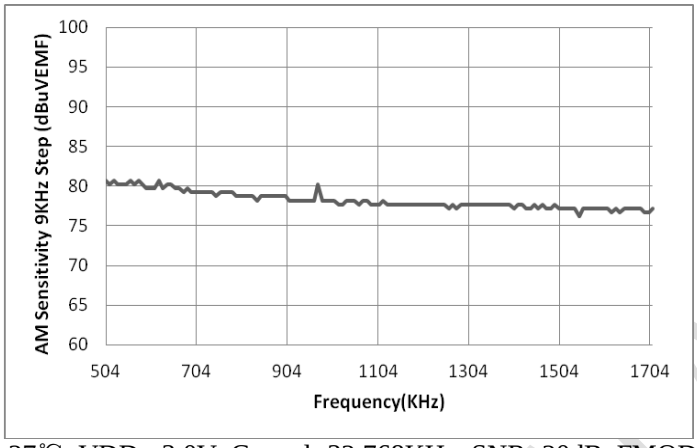


Test condition (Ta = 27℃, VDD= 3.0V, Crystal=32.768KHz, FMOD=1KHz, 75us de-emphasis, MONO=0, △F=75KHz,P_{in}=60dBuVEMF, Without weighting filter)

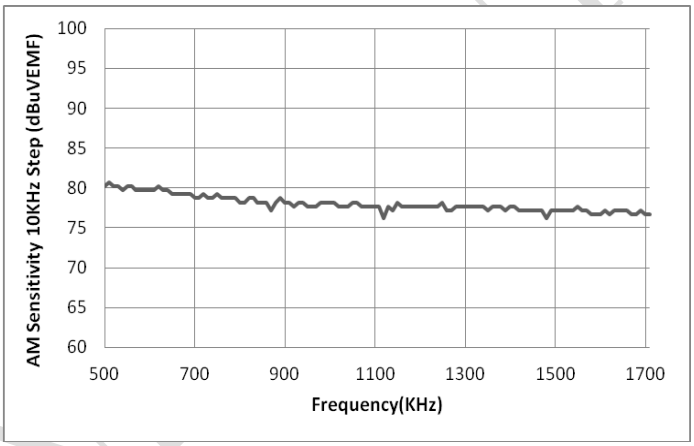


Test condition (Ta = 27℃, VDD= 3.0V, Crystal=32.768KHz, FMOD=1KHz, 75us de-emphasis, MONO=1, △F=22.5KHz,P_{in}=60dBuVEMF, Without weighting filter)

2.2. AM Characteristics



Test condition (Ta = 27℃, VDD= 3.0V, Crystal=32.768KHz, SNR=20dB, FMOD=1KHz,AM modulation index=30%,Without weighting filter, ferrite antenna =420uH,distance between Tx&Rx antenna=60cm)



Test condition (Ta = 27℃, VDD= 3.0V, Crystal=32.768KHz, SNR=20dB, FMOD=1KHz,AM modulation index=30%,Without weighting filter, ferrite antenna =420uH,distance between Tx&Rx antenna=60cm)

3. Pin List

Table 5: Pin list

Pin Index	Name	I/O Type	Description
1	AMINN	Analog Input	AM RF negative input.
2	AMINP	Analog Input	AM RF positive input.
3	RFINP	Analog Input	FM RF input.
4	RFGND	RF Ground	RF ground.
5	DVSS	Digital Ground	Digital ground.
6	DVDD	Digital Power	Digital power supply.
7	NC	NC	No connect.
8	ST	Digital Output	ST indicator.
9	SDA	Digital I/O	SDA of I^2C interface. Tied to an internal 47kohm pull-up resistor.
10	SCL	Digital I/O	SCL of I^2C interface. Tied to an internal 47kohm pull-up resistor.
11	ROUT	Analog Output	Right channel audio output.
12	LOUT	Analog Output	Left channel audio output.
13	AVSS	Analog Ground	Analog ground.
14	XTALN	Analog I/O	Crystal.
15	XTALP	Analog I/O	Crystal.
16	AVDD	Analog Power	Power supply.

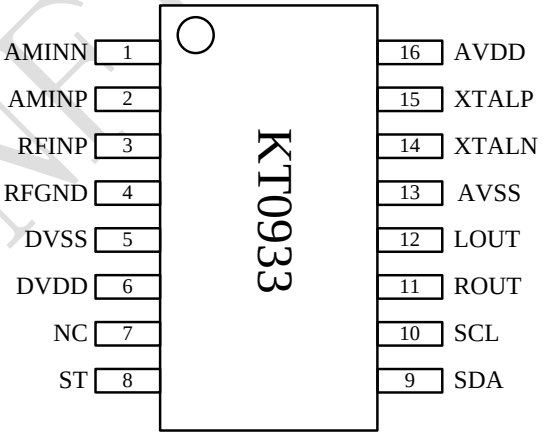


Figure 1：KT0933 Pin assignment (Top view)

4. Function Description

4.1. Overview

KT0933 offers a true single-chip, full-band FM/AM and versatile radio solution by minimizing the external components and offering a variety of configurations.

4.2. FM Receiver

KT0933 enters FM mode by setting register AM_FM to 0. The FM receiver is based on the architecture of KT Micro's latest generation FM receiver chips in mass production. There are no external filters or frequency-tuning devices thanks to a proprietary digital low-IF architecture consisting of a fully-integrated LNA, an automatic gain control (AGC), a set of high-performance ADCs, high-quality analog and digital filters, and an on-chip low-noise self-tuning VCO. The on-chip high-fidelity Class-AB driver further eliminates the need for external audio amplifiers and can drive stereo headphones directly.

4.3. AM Receiver

KT0933 enters AM mode by setting register AM_FM to 1. The AM Receiver employs a similar digital low IF architecture and share many circuits with the FM receiver. The minimum AM channel spacing can be set to 1KHz. The bandwidth of the channel filter can be set to 1KHz to 5KHz to suit various requirements.

The AM receiver in KT0933 can provide accurate and automatic AM tuning without manual alignment. It supports ferrite loop antenna with value between 360uH and 620uH.

4.4. Operation Bands

KT0933 supports wide FM band and AM bands. The FM receiver covers frequencies from 32MHz to 110MHz. The AM band is from 500KHz to 1750KHz.

4.5. Standby

To enter standby mode, the STDBY register shall be set to 1 through I^2C interface. To quit standby mode, STDBY should be set to 0.

4.6. Crystal and reference clock

KT0933 integrates a low frequency crystal oscillator that supports 32.768KHz or 38KHz crystals. Alternatively a CMOS level external reference clock may be used by setting the RCLK_EN register to 1 and setting FPFD<19:0> according to the frequency of the reference clock. The FPFD<19:0> is the frequency value in the unit of 1/16Hz. In order to illuminate the usage of these bits clearly some examples are given in Table 6.

Table 6: Examples using different crystal or reference clock

	RCLK_EN	FPFD<19:16>	FPFD<15:0>	DIVIDERP<10:0>	DIVIDERN<10:0>
32768Hz crystal	0	0x08	0x0000	0x0001	0x029C
38KHz crystal	0	0x09	0x4700	0x0001	0x0240
32.768KHz reference clock	1	0x08	0x0000	0x0001	0x029C
75KHz reference clock	1	0x09	0x27C0	0x0002	0x0247
4.2336 MHz reference clock	1	0x07	0x5499	0x008D	0x02D9
12MHz reference clock	1	0x07	0xD000	0x0177	0x02AC
24MHz reference clock	1	0x07	0xD000	0x02EE	0x02AC
40MHz reference clock	1	0x07	0xD000	0x04E2	0x02AC

4.7. Digital Signal Processing

4.7.1. FM Stereo Decoder

The digitized IF signal is fed to the FM demodulator which demodulates the signal and outputs a digital multiplexed (MPX) signal consisting of L+R audio, L-R audio, 19KHz pilot tone and RDS signal. The left channel signal and the right channel signal can be extracted from the MPX signal by simply adding and subtracting the L+R signal and L-R signal. The spectrum diagram is shown in Figure 2.

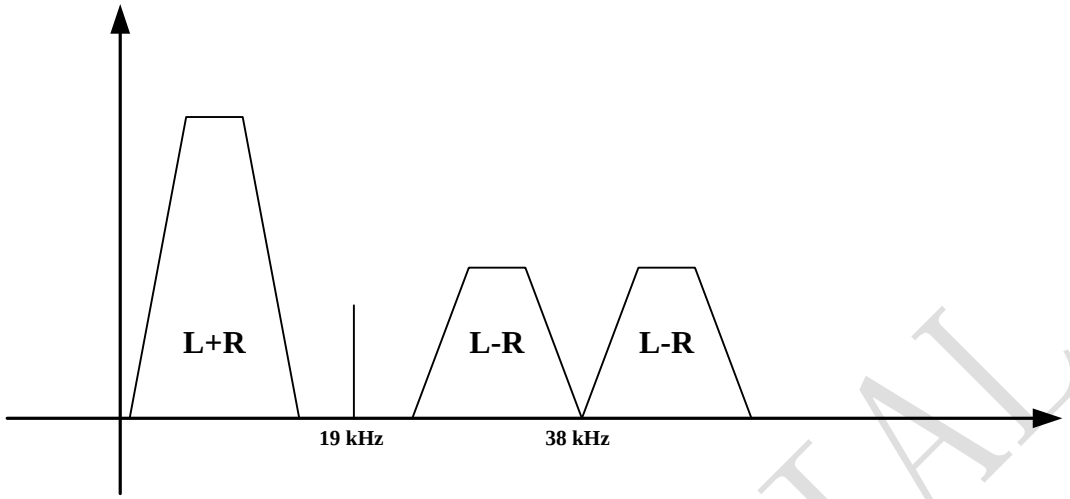


Figure 2: Spectrum diagram of the MPX signal

4.7.2. Mute / Softmute

KT0933 can be hard muted by setting VOLUME<4:0> to 0 and the output of the audio signal is set to the common mode voltage.

FM:
There is also a Soft Mute feature that is enabled by setting FM_DSMUTE to 0. In this mo de, the audio volume is gradually attenuated when the signal reception is weak. (i.e. when the RSSI or SNR is below a certain level defined by FM_SMUTE_START_RSSI<2:0> or FM_SMUTE_START _SNR<2:0>, respectively.) The attenuation slope can be config ured through FM_SMUTE_SLOPE_RSSI<2:0> or FM_SMUTE_SLOPE _SNR<2:0>, re spectively.
The maximum attenuation of volume is -21dB when RSSI is used as soft mute judgment t hreshold. The maximum attenuation of volume is -12dB when RSSI is used as soft mute j udgment threshold. The maximum total attenuation of volume can be configured through FM_SMUTE_MIN_GAIN<2:0>.

AM:
There is also a Soft Mute feature that is enabled by setting AM_DSMUTE to 0. In this m ode, the audio volume is gradually attenuated when the signal reception is weak. (i.e. whe n the RSSI and SNR are below a certain level as defined by AM_SMUTE_START_RSS I<2:0> or AM_SMUTE_START_ SNR<2:0>, respectively.) The attenuation slope can be configured through AM_SMUTE_SLOPE_ RSSI<2:0> or AM_SMUTE_SLOPE_SNR< 2:0>, respectively.
The maximum attenuation of volume is -21dB when RSSI is used as soft mute judgment threshold. The maximum attenuation of volume is -12dB when RSSI is used as soft mute

judgment threshold. The maximum total attenuation of volume can be configured through AM_SMUTE_MIN_GAIN<2:0>.

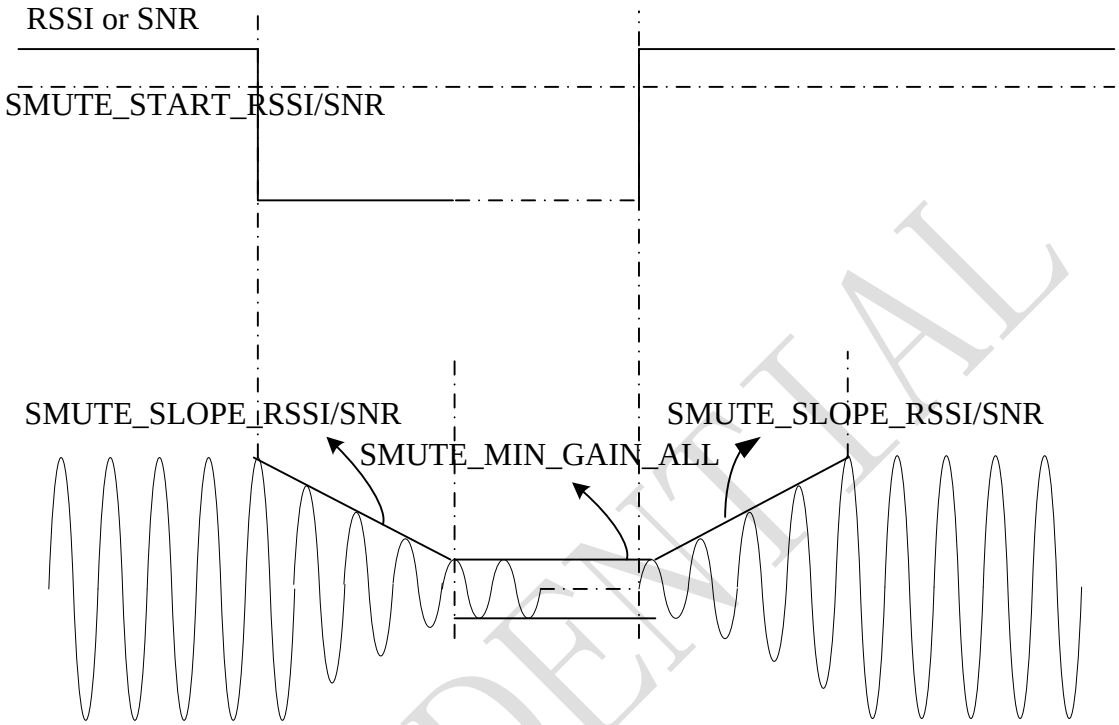


Figure 3: Softmute

4.7.3. Stereo / Mono Blending

In order to provide a comfortable listening experience, KT0933 blends the stereo signal with mono signal gradually when in weak reception in FM mode while the noise floor keep at the same level. The stereo separation starts increasing when the RSSI (SNR) of KT0933 grows up to the level defined by BLND_START_RSSI<3:0> (BLND_START_SNR<5:0>) and stop increasing when meets the level defined by the BLND_STOP_RSSI<3:0>(BLND_STOP_SNR<5:0>). The blending is disabled when DBLND is set to 1. BLND_MOD is used to select judgment condition: RSSI or SNR.
MONO playback mode can be forced by setting the MONO to 1.

4.7.4. Bass

KT0933 provides bass boost feature for audio enhancement. The gain of the bass boost can be programmed through BASS<1:0>. With BASS<1:0>=00, this feature is disabled.

4.7.5. Stereo DAC, Audio Filter and Driver

Two high-quality audio digital-to-analog converters (DAC) are integrated along with high-fidelity analog audio filters and class AB drivers. Headphones with impedance as low as 16ohms can be direct driven without adding external audio drivers. An integrated anti-pop circuit suppresses the click-and-pop sound during power up and power down.

In order to suit different applications, the gain of the audio driver can be adjusted through register bits FM_GAIN<2:0> , AM_GAIN<3:0>and AM_VOLUME<3:0>and to avoid the saturation in output stage, the common mode voltage can also be adjust according to different power supply voltage through register bits AUDV_DCLVL<2:0>.

4.7.6. AM Channel Filter Bandwidth

KT0933 provides programmable AM channel bandwidth from 1KHz to 5KHz through FLT_SEL <2:0>.

4.7.7. Tune

The fully integrated LO synthesizer supports wide band operation. Before tuning，the register of Channel should be written，and then write the register TUNE. Channel tuning is started when the register TUNE is set to 1.

In FM mode, the channel frequency is set by FM_CHAN<11:0> and is defined as

Freq(KHz) = 50KHz × FM_CHAN<11:0>

In AM mode, the channel frequency is set by AM_CHAN<14:0> and is defined as

Freq(KHz) = 1KHz × AM_CHAN<14:0>

4.7.8. SEEK

KT0933 offers effective software based seek algorithm. Refer to application notes for more information.

4.8. I²C Control Interface

Write Operations:

BYTE WRITE:

The write operation is accomplished via a 3-byte sequence:

Serial address with write command
Register address
Register data

A write operation requires an 8-bit register address following the device address word and acknowledgment. Upon receipt of this address, the KT0933 will again respond with a "0" and then clock in the 8-bit register data. Following receipt of the 8-bit register data, the KT0933 will output a "0" and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition (see Figure 4).

Read Operations:

RANDOM READ:

The read operation is accomplished via a 4-byte sequence:

Serial address with write command
Register address
Serial address with read command
Register data

Once the device address and register address are clocked in and acknowledged by the KT0933, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The KT0933 acknowledges the device address and serially clocks out the register data. The microcontroller does not respond with a "0" but does generate a following stop condition (see Figure 4).

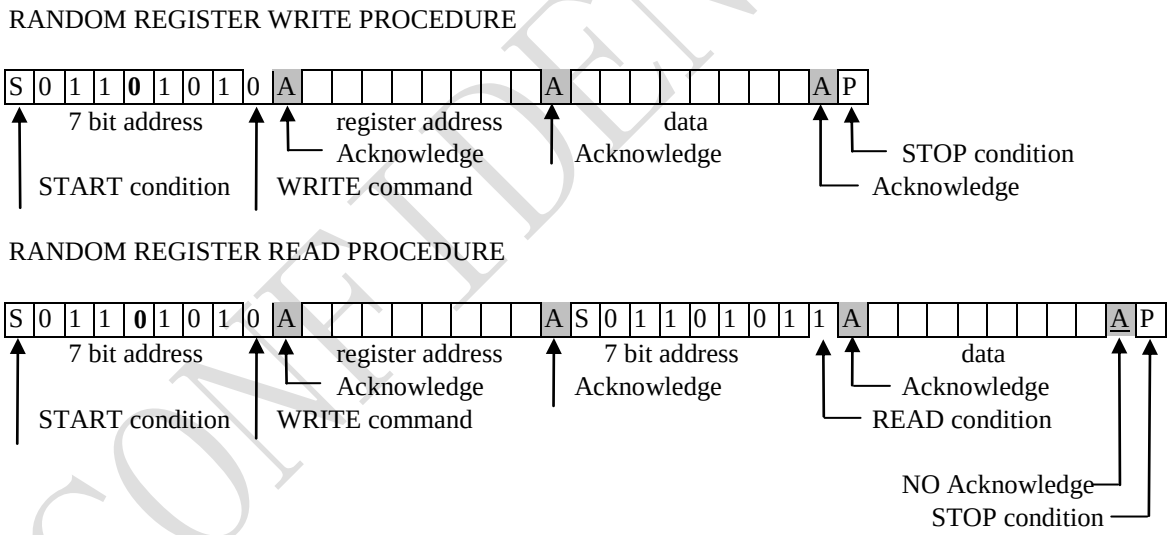


Figure 4: Serial Interface Protocol

CURRENT ADDRESS READ: The internal data register address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained.

Once the device address with the read/write select bit set to "1" is clocked in and acknowledged by the KT0933, the current address data word is serially clocked out. The microcontroller does not respond with an input "0" but does generate a following stop condition (see Figure 5).

CURRENT REGISTER READ
PROCEDURE

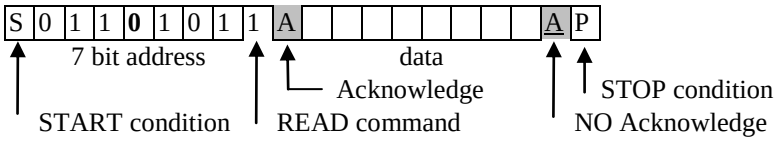


Figure 5: Serial Interface Protocol

Note: The serial controller supports slave mode only. Any register can be addressed randomly.

The address of the slave in the first 7 bits and the 8th bit tells whether the master is receiving data from the slave or transmitting data to the slave. The I^2C write address is 0x6C and the read address is 0x6D.

CLOCK and DATA TRANSITIONS: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see Figure6). Data changes during SCL high periods will indicate a start or stop condition as defined below.

START CONDITION: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (see Figure gure 7).

STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the KT0933 in a standby power mode (see Figure 7).

ACKNOWLEDGE: All addresses and data words are serially transmitted to and from the KT0933 in 8-bit words. The KT0933 sends a "0" to acknowledge that it has received each word. This happens during the ninth clock cycle (see Figure 8).

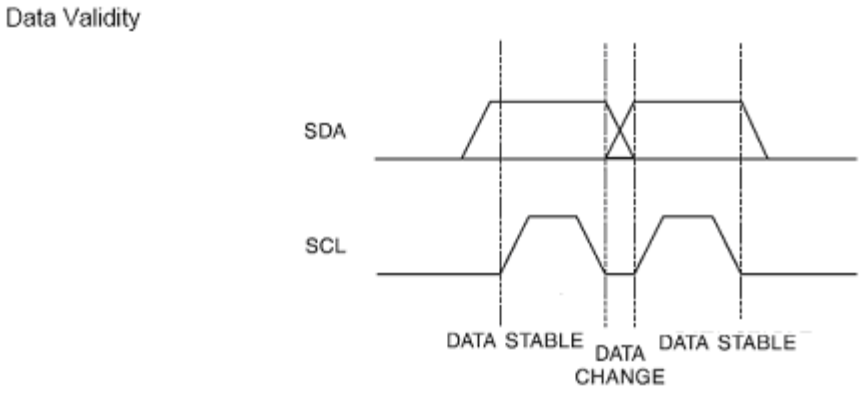


Figure 6: Clock and Data Transitions

Start and Stop Definition

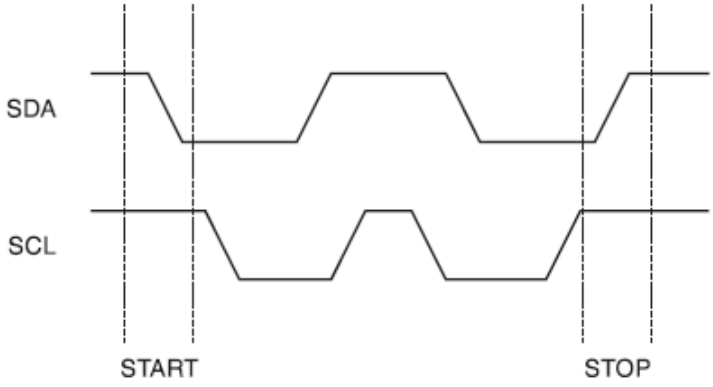


Figure 7: Start and Stop Definition

Output Acknowledge

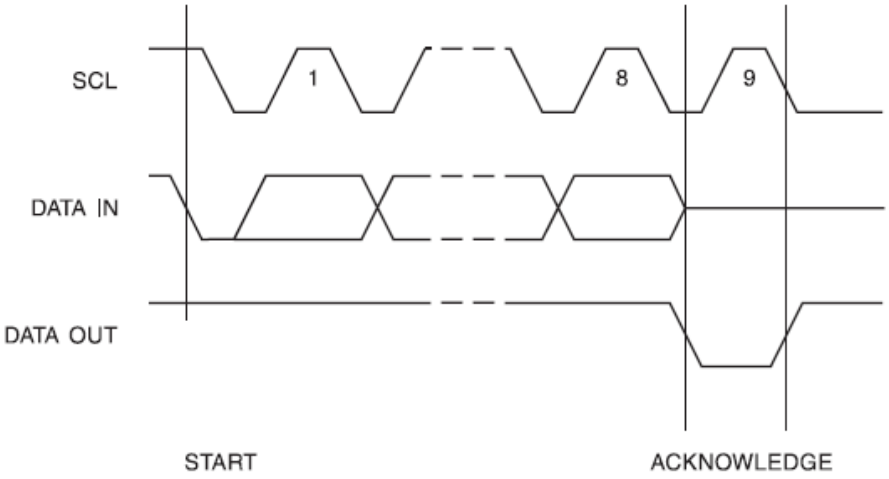


Figure 8: Acknowledge

4.9. Register Bank

4.9.1. DEVICEID0 (Address 0x0000)

Bit	Name	Access	Default Value	Functional Description
7:0	Device ID0	R	0x82	

4.9.2. DEVICEID1 (Address 0x0001)

Bit	Name	Access	Default Value	Functional Description
7:0	Device_ID1	R	0x06	

4.9.3. KTMARK0 (Address 0x0002)

Bit	Name	Access	Default Value	Functional Description
7:0	KT_Mark0	R	0x4B	ASCII form of string “K”

4.9.4. KTMARK1 (Address 0x0003)

Bit	Name	Access	Default Value	Functional Description
7:0	KT_Mark1	R	0x54	ASCII form of string “T”

4.9.5. PLLCFG0 (Address 0x0004)

Bit	Name	Access	Default Value	Functional Description
7	SYS_CFGOK	RW	0	Clock initialization completed
6:3	Reserved	RW	000_0	Reserved
2:0	DIVIDERP<10:8>	RW	000	**PLL divider P configuration.**

4.9.6. PLLCFG1 (Address 0x0005)

Bit	Name	Access	Default Value	Functional Description
7:0	DIVIDERP<7:0>	RW	1	**PLL divider P configuration.**

4.9.7. PLLCFG2 (Address 0x0006)

Bit	Name	Access	Default Value	Functional Description
7:3	Reserved	RW	0	
2:0	DIVIDERN<10:8>	RW	010	**PLL divider N configuration.**

4.9.8. PLLCFG3 (Address 0x0007)

Bit	Name	Access	Default Value	Functional Description
7:0	DIVIDERN<7:0>	RW	1001_1100	**PLL divider N configuration.**

4.9.9. SYSCLK_CFG0 (Address 0x0008)

Bit	Name	Access	Default Value	Functional Description
7:4	Reserved	RW	0000	Reserved
3:0	FPFD<19:16>	RW	1000	Phase-detection frequency. FPFD<19:0> = External Xtal clock or RCLK frequency / DIVIDERP

4.9.10. SYSCLK_CFG1 (Address 0x0009)

Bit	Name	Access	Default Value	Functional Description
7:0	FPFD<15:8>	RW	0x00	Phase-detection frequency. FPFD<19:0> = External Xtal clock or RCLK frequency / DIVIDERP

4.9.11. SYSCLK_CFG2 (Address 0x000A)

Bit	Name	Access	Default Value	Functional Description
7:0	FPFD<7:0>	RW	0x00	Phase-detection frequency. FPFD<19:0> = External Xtal clock or RCLK frequency / DIVIDERP

4.9.12. XTALCFG (Address 0x000d)

Bit	Name	Access	Default Value	Functional Description
7:5	Reserved	RW	110	
4	RCLK_EN	RW	0	**Reference clock enable.** 0 = Crystal 1 = External reference clock.
3:0	Reserved	RW	011	

4.9.13. RXCFG0 (Address 0x000e)

Bit	Name	Access	Default Value	Functional Description
7:6	Reserved	RW	00	
5	STDBY	RW	0	**Standby mode control.** 0 = Normal operation 1 = Standby mode.
4:0	Reserved	RW	0_0000	

4.9.14. RXCFG1 (Address 0x000f)

Bit	Name	Access	Default Value	Functional Description
7:5	Reserved	R	000	
4:0	VOLUME<4:0>	RW	1_1111	Volume control bits: 11111 = 0dB 11110 = -2dB 11101 = -4dB …… 00010 = -58dB 00001 = -60dB 00000 = mute

4.9.15. BANDCFG3 (Address 0x0019)

Bit	Name	Access	Default Value	Functional Description
7:5	AM_SMUTE_MIN_GAIN<2:0>	RW	0	The total attenuation of volume can be configured: 000 = -9dB 001 = -12dB 010 = -15dB 011 = -18dB 100 = -21dB 101 = -24dB 110 = -27dB 111 = -30dB
4:2	FM_SMUTE_MIN_GAIN<2:0>	RW	0	The total attenuation of volume can be configured: 000 = -9dB 001 = -12dB 010 = -15dB 011 = -18dB 100 = -21dB 101 = -24dB 110 = -27dB 111 = -30dB
1:0	Reserved	RW	00	

4.9.16. MUTECFG0 (Address 0x001a)

Bit	Name	Access	Default Value	Functional Description
7	FM_DSMUTE	RW	0	FM Softmute Disable 0 = FM softmute enable 1 = FM softmute disable
6	AM_DSMUTE	RW	0	AM Softmute Disable 0 = AM softmute enable 1 = AM softmute disable
5	DMUTER	RW	1	Right channel mute control 0 = Mute enable 1 = Mute disable

Bit	Name	Access	Default Value	Functional Description
4	DMUTEL	RW	1	Left channel mute control 0 = Mute enable 1 = Mute disable
3:0	Reserved	R	1000	

4.9.17. G38KCFG0 (Address 0x001b)

Bit	Name	Access	Default Value	Functional Description
7:3	Reserved	RW	0000_0	
2	POWERON_FINISH	RW	0	Power On Flow Finish Flag 0 = Initialization 1 = Finish
1:0	Reserved	RW	0	

4.9.18. SOFTMUTE0 (Address 0x001d)

Bit	Name	Access	Default Value	Functional Description
7	Reserved	RW	0	
6:0	AM_SMUTE_START_ RSSI<6:0>	RW	0	

4.9.19. SOFTMUTE1 (Address 0x001e)

Bit	Name	Access	Default Value	Functional Description
7:3	Reserved	RW	0000_0	
2:0	AM_SMUTE_SLOPE_ RSSI<2:0>	RW	0	The attenuation slope can be configured 000=4 001=3 010=2 011=1 100=1/2 101=1/3 110=1/4 111=0

4.9.20. SOFTMUTE2 (Address 0x001f)

Bit	Name	Access	Default Value	Functional Description
7	Reserved	RW	0	
6:4	FM_SMUTE_START_ RSSI<2:0>	RW	0	The attenuation start level can be configured throgh 000=22 dBuVEMF 001=20 dBuVEMF 010=18 dBuVEMF 011=16 dBuVEMF 100=14 dBuVEMF 101=12 dBuVEMF 110=10 dBuVEMF 111=8dBuVEMF

3	Reserved	RW	0	
2:0	FM_SMUTE_SLOPE_ RSSI<2:0>	RW	0	The attenuation slope can be configured 000=4 001=3 010=2 011=1 100=1/2 101=1/3 110=1/4 111=0

4.9.21. SOFTMUTE3 (Address 0x0020)

Bit	Name	Access	Default Value	Functional Description
7	Reserved	RW	0	
6:0	AM_SMUTE_START_ SNR<6:0>	RW	0	

4.9.22. SOFTMUTE4 (Address 0x0021)

Bit	Name	Access	Default Value	Functional Description
7	Reserved	RW	0	
6:4	AM_SMUTE_SLOPE_ SNR<2:0>	RW	0	The attenuation slope can be configured 000=4 001=3 010=2 011=1 100=1/2 101=1/3 110=1/4 111=0
3	Reserved	RW	0	
2:0	FM_SMUTE_SLOPE_ SNR<2:0>	RW	0	The attenuation slope can be configured 000=4 001=3 010=2 011=1 100=1/2 101=1/3 110=1/4 111=0

4.9.23. SOFTMUTE5 (Address 0x0022)

Bit	Name	Access	Default Value	Functional Description
7:6	Reserved	RW	0	
5:0	FM_SMUTE_START_ SNR<5:0>	RW	0	FM softmute

4.9.24. SOUNDCFG (Address 0x0028)

Bit	Name	Access	Default Value	Functional Description
7:6	Reserved	R	00	
5:4	BASS<1:0>	RW	00	Bass boost effect mode selection 00 = Bypass 01 = 9.4 dB@70Hz 10 = 13.3dB@70Hz 11 = 18.2dB@70Hz
3:0	Reserved	RW	1101	

4.9.25. FLT_CFG (Address 0x0029)

Bit	Name	Access	Default Value	Functional Description
7:5	Reserved	RW	000	
4	BLND_MOD	RW	0	Blend Mode Selection 0 = RSSI mode 1 = SNR mode
3:0	Reserved	R	00000	

4.9.26. DSPCFG0 (Address 0x002a)

Bit	Name	Access	Default Value	Functional Description
7	Reserved	RW	0	Reserved
6:4	FM_GAIN<2:0>	RW	000	Audio gain for FM audio processor. 000 = 0dB 001 = 3.5dB 010 = 6dB 011 = 9.5dB 100 = -2.5dB 101 = -3.66dB 110 = -6dB 111 = -8.5dB
3:0	Reserved	RW	0000	

4.9.27. DSPCFG1 (Address 0x002b)

Bit	Name	Access	Default Value	Functional Description
7	MONO	RW	0	Mono Selection 0 = Stereo 1 = Force mono
6:4	Reserved	RW	00	
3	DE	RW	0	**De-emphasis Time Constant Selection.** 0 = 75us. Used in USA. 1 = 50us. Used in Europe, Australia, Japan.
2:1	Reserved	RW	00	
0	DBLND	RW	0	Blend Disable 0 = Blend enable

Bit	Name	Access	Default Value	Functional Description
				1 = Blend disable

4.9.28. DSPCFG2 (Address 0x002c)

Bit	Name	Access	Default Value	Functional Description
7:4	BLND_START_RSSI<3:0>	RW	0000	0000=8dbuVEMF 0001=10dbuVEMF 0010=12dbuVEMF 0011=14dbuVEMF 0100=16dbuVEMF 0101=18dbuVEMF 0110=20dbuVEMF 0111=22dbuVEMF 1000=24dbuVEMF 1001=26dbuVEMF 1010=28dbuVEMF 1011=30dbuVEMF 1100=32dbuVEMF 1101=34dbuVEMF 1110=36dbuVEMF 1111=38dbuVEMF
3:0	BLND_STOP_RSSI<3:0>	RW	0000	0000=8dbuVEMF 0001=10dbuVEMF 0010=12dbuVEMF 0011=14dbuVEMF 0100=16dbuVEMF 0101=18dbuVEMF 0110=20dbuVEMF 0111=22dbuVEMF 1000=24dbuVEMF 1001=26dbuVEMF 1010=28dbuVEMF 1011=30dbuVEMF 1100=32dbuVEMF 1101=34dbuVEMF 1110=36dbuVEMF 1111=38dbuVEMF

4.9.29. DSPCFG6 (Address 0x0030)

Bit	Name	Access	Default Value	Functional Description
7:5	Reserved	RW	101	
4:0	FM_RSSI_BIAS<4:0>	RW	0_0000	10000 = -16dB 10001 = -15dB …… 11110 = -2dB 11111 = -1dB 00000 = 0dB 00001 = 1dB ……

				01111 = 15dB

4.9.30. EMC_CFG0 (Address 0x0031)

Bit	Name	Access	Default Value	Functional Description
7:6	Reserved	RW	01	
5	EMC_EN	RW	1	EMC enable. 0 = Disable. 1 = Enable.
4:0	Reserved	RW	0_1011	

4.9.31. DSPCFG7 (Address 0x0034)

Bit	Name	Access	Default Value	Functional Description
7:6	Reserved	R	0	
5:0	BLEND_START_SNR<5:0>	RW	0	When the starting value meets the ending value, that is separated immediately.

4.9.32. DSPCFG8 (Address 0x0035)

Bit	Name	Access	Default Value	Functional Description
7:6	Reserved	R	0	
5:0	BLEND_STOP_SNR<5:0>	RW	0	When the starting value meets the ending value, that is separated immediately.

4.9.33. AFC2 (Address 0x003e)

Bit	Name	Access	Default Value	Functional Description
7	Reserved	RW	0	
6	FM_AFCD	RW	0	AFC disable control bit 0 = AFC enable 1 = AFC disable
5:3	Reserved	RW	000	
2:0	FM_TH_AFC<2:0>	RW	111	Programmable threshold for FM AFC △F digital IF offset that can be adjusted in FM mode. 000 = 5k 001= 15k 010 = 25k 011= 35k 100= 50k 101 =100k 110= 150k 111= 200k

4.9.34. AFC3 (Address 0x003f)

Bit	Name	Access	Default Value	Functional Description
7	Reserved	RW	0	
6	AM_AFCD	RW	0	AFC disable control bit 0 = AFC enable 1 = AFC disable
5:3	Reserved	RW	000	
2:0	AM_TH_AFC <2:0>	RW	000	**AM AFC Threshold.** 000= 23*2^7 001= 39*2^7 010= 47*2^7 011= 63*2^7 100= 78*2^7 101= 94*2^7 110= 117*2^7 111= 127*2^7

4.9.35. ANACFG (Address 0x004e)

Bit	Name	Access	Default Value	Functional Description
7:6	Reserved	RW	00	
5:4	DEPOP_TC <1:0>	RW	00	De-pop time constant. 00 = 250ms 01 = 500ms 10 = 750ms 11 = 1s
3	Reserved	RW	0	
2:0	AUDV_DCLVL <2:0>	RW	101	Audio Output Common Voltage: 000= 0.85v 001=0.91v 010= 1.05v 011= 1.15v 100= 1.20v 101= 1.35v 110= 1.50v 111=1.60v

4.9.36. AMCALI0 (Address 0x0055)

Bit	Name	Access	Default Value	Functional Description
7:3	Reserved	RW	0000_0	
2:0	AM_Q <2:0>	RW	100	AM Antenna Q factor control 000 = Minimum Q factor …… 111 = Maximum Q factor

4.9.37. AMDSP0 (Address 0x0062)

Bit	Name	Access	Default Value	Functional Description
7:4	AM_GAIN<3:0>	RW	0110	**Audio gain for AM audio processor.** 0000 = 6dB 0001 = 3dB 0010 = 0dB 0011 = -3dB 0100 = -6dB 0101 = -9dB 0110 = -12dB 0111 = -15dB 1000 = -18dB
3	Reserved	R	0	
2:0	FLT_SEL<2:0>	RW	001	AM Channel Filter Bandwidth Selection, 000=1.2KHz 001=2.4KHz 010=3.6KHz 011=4.8KHz 100=6.0KHz

4.9.38. AMDSP1 (Address 0x0063)

Bit	Name	Access	Default Value	Functional Description
7:5	Reserved	RW	000	
4:0	AM_RSSI_BIAS<4:0>	RW	0_0000	AM RSSI offset

4.9.39. AMDSP4 (Address 0x0066)

Bit	Name	Access	Default Value	Functional Description
7:3	Reserved	R	0001_0	
2:0	AM_SNR_MODE_SEL<2:0>	RW	000	AM SNR Mode Selection: 000= AM_SNR_MODE1 001= AM_SNR_MODE2 010= AM_SNR_MODE2 011= AM_SNR_MODE2 100= Reserved 101= Reserved 110= Reserved 111:=Reserved

4.9.40. AMDSP7 (Address 0x0069)

Bit	Name	Access	Default Value	Functional Description
7:4	Reserved	RW	1000	
3:0	AM_VOLUME<3:0>	RW	1110	AM Volume Control bits: 1111=0dB 1110= -0.5dB 1101=-1.0dB 1100= -1.5dB 1011= -2.0dB 1010= -2.5dB 1001= -3.0dB 1000= -3.5dB 0111= -4.0dB 0110= -4.5dB 0101= -5.0dB 0100= -5.5dB 0011= -6.0dB 0010= -6.5dB 0001= -7.0dB 0000= -7.5dB

4.9.41. STATUS10 (Address 0x0079)

Bit	Name	Access	Default Value	Functional Description
7:0	AFC_AAF<7:0>	R	0	AFC Accumulative Adjust Frequency. FM mode: 0x80 = -128*2048Hz 0x81 = -127*2048Hz …… 0xFF = -1*2048Hz 0x00 = 0Hz 0x01 = 1*2048Hz …… 0x7E=126*2048Hz 0x7F = 127 *2048Hz AM mode: 0x80 = -128*128Hz 0x81 = -127*128Hz …… 0xFF = -1*128Hz 0x00 = 0Hz 0x01 = 1*128Hz …… 0x7E=126*128Hz 0x7F = 127 *128Hz

4.9.42. SPARE0 (Address 0x0085)

Bit	Name	Access	Default Value	Functional Description
7:6	Reserved	RW	00	
5:0	FM_DELTN_INTERF<5:0>	RW	00_0000	**To remove interference on appointed FM CHAN frequency, the system clock PLL DIVIDERN will increase / decrease number.**

4.9.43. FMCHAN0 (Address 0x0088)

Bit	Name	Access	Default Value	Functional Description
7	TUNE	RW	0	FM or AM Tune enable. 0 = Normal operation 1 = Tune process is enable. This bit will automatically clear 0 after tune process.
6	AM_FM	RW	1	**AM/FM mode switching.** 0 = FM mode. 1 = AM mode.
5:4	Reserved	R	00	
3:0	FM_CHAN<11:8>	RW	0110	**FM channel with 50KHz step.** Frequency(KHz)=FM_CHAN<11:0>*50KHz Default is 0x06B8(86MHz)

4.9.44. FMCHAN1 (Address 0x0089)

Bit	Name	Access	Default Value	Functional Description
7:0	FM_CHAN<7:0>	RW	1011_1000	**FM channel with 50KHz step.** Frequency(KHz)=FM_CHAN<11:0>*50KHz Default is 0x06B8(86MHz)

4.9.45. AMCHAN0 (Address 0x008c)

Bit	Name	Access	Default Value	Functional Description
7	Reserved	R	0	
6:0	AM_CHAN<14:8>	RW	001	**AM channel with 1KHz step.** Frequency(KHz) = AM_CHAN<11:0>*1KHz Default is 0x01F8 (504KHz)

4.9.46. AMCHAN1 (Address 0x008d)

Bit	Name	Access	Default Value	Functional Description
7:0	AM_CHAN<7:0>	RW	1111_1000	**AM channel with 1KHz step.** Frequency(KHz) = AM_CHAN<11:0>*1KHz Default is 0x01F8 (504KHz)

4.9.47. STATUS0 (Address 0x00de)

Bit	Name	Access	Default Value	Functional Description
7:3	Reserved		0000_0	
2	VALID_TUNE	RW	0	**Valid channel indicator.** 0 = Invalid channel. 1 = Valid channel.
1	Reserved		0	
0	ST	RW	0	Stereo indicator 0 = MONO state 1 = Stereo state

4.9.48. STATUS4 (Address 0x00e2)

Bit	Name	Access	Default Value	Functional Description
7:6	Reserved	R	0	
5:0	FMSNR<5:0>	R	0	Channel SNR value is FM mode. 000000 = minimum SNR …… 111111 = maximum SNR

4.9.49. STATUS6 (Address 0x00e4)

Bit	Name	Access	Default Value	Functional Description
7	Reserved	R	0	
6:0	RDCHAN<14:8>	RW	0x06	**Current Channel Indicator.** FM mode: Frequency(KHz) = RDCHAN<11:0>*50KHz AM mode: Frequency(KHz) = RDCHAN<11:0>*1KHz

4.9.50. STATUS7 (Address 0x00e5)

Bit	Name	Access	Default Value	Functional Description
7:0	RDCHAN<7:0>	RW	0xb8	**Current Channel Indicator.** FM mode: Frequency(KHz) = RDCHAN<11:0>*50KHz AM mode: Frequency(KHz) = RDCHAN<11:0>*1KHz

4.9.51. STATUS8 (Address 0x00e6)

Bit	Name	Access	Default Value	Functional Description
7	Reserved	R	0	
6:0	FMRSSI<6:0>	R	0000000	FM RSSI value indicator. FM RSSI(dBm)=-110 + FM RSSI<6:0> * 1dB

4.9.52. AFC_STATUS0 (Address 0x00e8)

Bit	Name	Access	Default Value	Functional Description
7:0	AM_CARRIER_OFST <7:0>	R	0x00	**AM carrier frequency offset.** 0x80 = -128*128Hz 0x81 = -127*128Hz …… 0xFF = -1*128Hz 0x00 = 0 0x01 = 1*128Hz …… 0x7E=126*128Hz 0x7F = 127 *128Hz

4.9.53. AFC_STATUS1 (Address 0x00e9)

Bit	Name	Access	Default Value	Functional Description
7:0	FM_CARRIER_OFST <7:0>	R	0x00	**AM carrier frequency offset.** 0x80 = -128*1024Hz 0x81 = -127*1024Hz …… 0xFF = -1*1024Hz 0x00 = 0Hz 0x01 = 1*1024Hz …… 0x7E=126*1024Hz 0x7F = 127 *1024Hz

4.9.54. AMSTATUS0 (Address 0x00ea)

Bit	Name	Access	Default Value	Functional Description
7	Reserved	R	0	
6:0	AMRSSI<6:0>	R	000_0000	AM RSSI value indicator. AM RSSI(dBm)=-110+ AMRSSI<6:0> *1dB

4.9.55. AMSTATUS2 (Address 0x00ec)

Bit	Name	Access	Default Value	Functional Description
7	Reserved	R	00	
6:0	AM_SNR_MODE 1<6:0>	R	000_0000	AM Channel SNR value (Mode 1). 000000 = minimum SNR …… 111111 = maximum SNR

4.9.56. AMSTATUS3 (Address 0x00ed)

Bit	Name	Access	Default Value	Functional Description
7	AM_CARRY_LOCK	R	0	AM Carry Frequency Lock Flag: 0 = Lock loses. 1 = Lock.
6:0	AM_SNR_MODE 2<6:0>	R	000_0000	AM Channel SNR value (Mode 2). 000000 = minimum SNR …… 111111 = maximum SNR When AM_SNR_MODE_SEL=1/2/3, AM_SNR_MODE2 is valid.

5. Typical Application Circuit

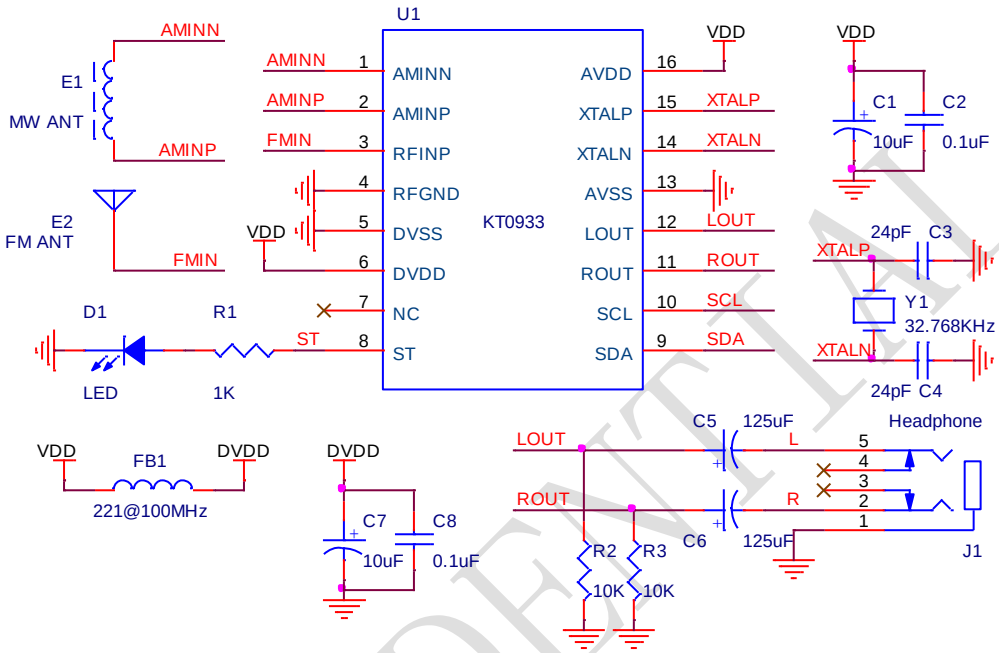
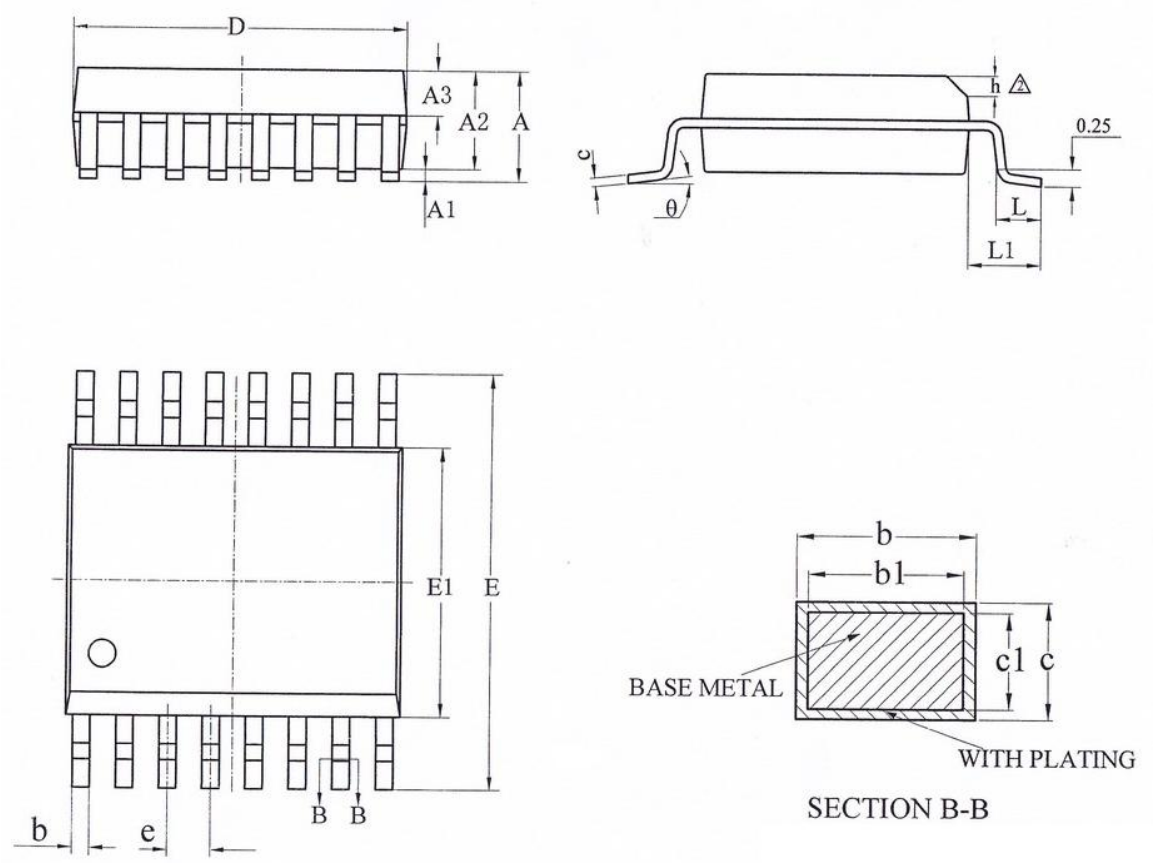


Figure 9: Typical application circuits

Components	Description	Value/Suppliers
C1,C7	Supply decoupling capacitor	10uF
C2,C8	Supply decoupling capacitor	0.1uF
C3,C4	Crystal load capacitor	24pF
C5,C6	AC coupling capacitor	125uF
D1	ST indicator	LED
E1	MW ferrite antenna	420uH
E2	FM antenna	
FB1	Ferrite bead	221@100MHz
J1	Headphone Jack	
R1	Resistor	1Kohm
R2,R3	Resistor	10Kohm
U1	AM/FM Receiver	KT0933
Y1	Crystal	32.768KHz

6. Package Outline



Symbol	Dimensions In Millimeters		
	Min.	Nom.	Max.
A	-	-	1.75
A1	0.10	-	0.225
A2	1.30	1.40	1.50
A3	0.50	0.60	0.70
b	0.24	-	0.30
b1	0.23	0.254	0.28
c	0.20	-	0.25
c1	0.19	0.20	0.21
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	-	4.00
e	0.635BSC		
h	0.25	-	0.50
L	0.50	0.65	0.80
L1	1.05BSC		
θ	0 °	-	8 °

7. Order Information

Part number	Description	Package	MOQ
KT0933	3rd generation monolithic digital AM/FM receiver	SSOP16L(0.635-D1.4), Pb free	2500 pcs

8. Revision History

V1.0 Firstly Release.
V1.1 Modified Electrical specification, Typical performance characteristics.
V1.2 Modified Function description.
V1.3 Modified Typical performance characteristics.

9. Contact Information

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